# Crystal Oscillator (SPXO)

· Package size (2.5 mm × 2.0 mm × 0.74 mm)
· Fundamental mode SPXO
· Output: CMOS
· Reference weight Typ.12 mg

## [ 1 ] Product Number / Product Name

(1-1) Product Number / Ordering Code

**X1G0061910025xx**

Last 2 digits code(**xx**) defines Quantity.
The standard is "16", 3 000 pcs/Reel.

(1-2) Product Name / Model Name

**SG-8201CG 98.304000 MHz TBHPA**

## [ 2 ] Operating Range

| Parameter | Symbol | Specifications | | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Supply voltage | $V_{CC}$ | 1.62 | - | 3.63 | V | - |
| | GND | 0 | 0 | 0 | V | - |
| Operating temperature range | T_use | -40 | +25 | +105 | °C | - |
| CMOS load condition | L_CMOS | - | - | 15 | pF | - |

## [ 3 ] Frequency Characteristics

(Unless stated otherwise [ 3 ] Operating Range)

| Parameter | Symbol | Specifications | | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Output frequency | fo | - | 98.304000 | - | MHz | - |
| Frequency tolerance *1 | f_tol | -15 | - | +15 | $\times 10^{-6}$ | T_use |

*1 Frequency tolerance includes Initial frequency tolerance, Frequency / temperature characteristics, Frequency / voltage coefficient Frequency / load coefficient and frequency aging (+25 °C. First year)

## [ 4 ] Electrical Characteristics

(Unless stated otherwise [ 3 ] Operating Range)

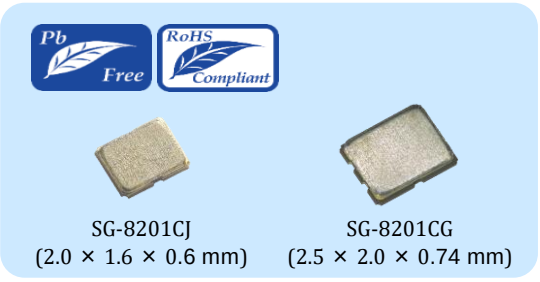
| Parameter | Symbol | Specifications | | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Start-up time | t_str | - | - | 3 | ms | t = 0 at 90 % Vcc |
| Current consumption | $I_{CC}$ | - | 7.9 | 10.4 | mA | No load condition, Vcc = 3.3 V |
| Disable current | I_dis | - | 5.1 | 7.4 | mA | OE = GND, Vcc = 3.3 V |
| Output voltage | $V_{OH}$ | 90 % $V_{CC}$ | - | - | V | $I_{OH}$ = -1 mA |
| | $V_{OL}$ | - | - | 10 % $V_{CC}$ | V | $I_{OL}$ = 1 mA |
| Rise/Fall time | tr/tf | - | - | 2.5 | ns | 20 % - 80 % Vcc level, L_CMOS = 15 pF |
| Symmetry | SYM | 45 | - | 55 | % | 50 % Vcc level, L_CMOS ≤ 15 pF |
| Input voltage | $V_{IH}$ | 70 % $V_{CC}$ | - | - | V | #1 pin |
| | $V_{IL}$ | - | - | 30 % $V_{CC}$ | V | #1 pin |
| Output disable time (OE) | tstp_oe | - | - | 1 | µs | Measured from the time OE pin crosses 30 % Vcc |
| Output enable time (OE) | tsta_oe | - | - | 100 ns + 2 clock cycles | - | Measured from the time OE pin crosses 70 % Vcc |
| Phase jitter | $t_{PJ}$ | - | - | - | ps | - |

**[ For other general specifications, please refer to the attached Full Data Sheet below ]**

# Low Jitter Programmable* Crystal Oscillator: SG-8201CJ, SG-8201CG

## Features

- Crystal oscillator (Programmable*)
- Output frequency: 1.2 MHz to 170 MHz
- Output: CMOS
- Supply voltage: 1.62 V to 3.63 V
- Frequency tolerance, Operating temperature:
  ±15 × $10^{-6}$ / -40 °C to +105 °C
  ±25 × $10^{-6}$ / -40 °C to +125 °C
- Phase jitter: 1.1 ps Typ.
  (Offset freq.: 12 kHz to 20 MHz, fo = 125 MHz)

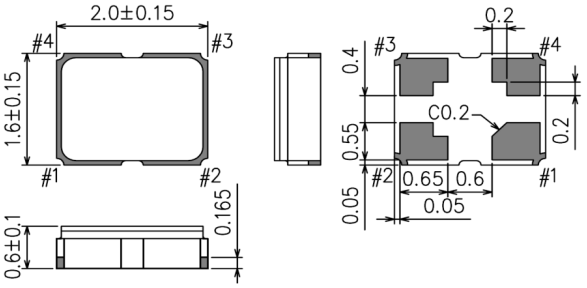



## Description

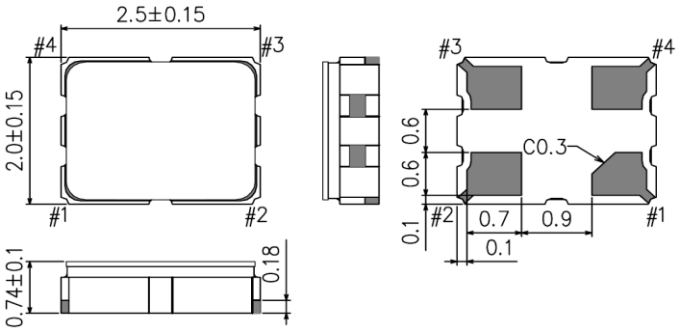
SG-8201CJ and SG-8201CG utilize Epson's new low noise fractional-N PLL technology, where the stability has been improved by ~2x and phase jitter has been reduced <1/25th versus the previous generation of Epson's programmable* crystal oscillator.
SG-8201CJ and SG-8201CG can be programmed to any frequency from 1.2 MHz to 170 MHz, with wide operating temperature range up to 125°C.
SG-8201CJ and SG-8201CG are ideal for variety of consumer and industrial applications, which requires small form factor and/or operation in harsh environment.

## Outline Drawing and Terminal Assignment

SG-8201CJ




SG-8201CG




Terminal Assignment

| Pin # | Name | Function | | |
|---|---|---|---|---|
| #1 | OE | Output Enable | High*1 or Open: | Specified frequency output from OUT pin |
| | | | Low: | OUT pin is low (pull down with 500 kΩ), only output driver is disabled |
| | $\overline{OE}$ | Output Enable | Low*2 or Open: | Specified frequency output from OUT pin |
| | | | High: | OUT pin is low (pull down with 500 kΩ), only output driver is disabled |
| | $\overline{ST}$ | Standby | High*1 *3: | Specified frequency output from OUT pin |
| | | | Low: | OUT pin is low (pull down with 500 kΩ)<br>Device goes to standby mode. Supply current reduces to the least as I_std |
| | ST | Standby | Low*2 *3: | Specified frequency output from OUT pin |
| | | | High: | OUT pin is low (pull down with 500 kΩ)<br>Device goes to standby mode. Supply current reduces to the least as I_std |
| #2 | GND | Ground | | |
| #3 | OUT | Clock output | | |
| #4 | $V_{CC}$ | Power supply | | |

*1 If fixing it at High, please connect to $V_{CC}$ directly.
*2 If fixing it at Low , please connect to GND directly.
*3 If necessary to use Open, please select Output Enable function.

* Programming with new writer is expected to be available from 2025.

[ 1 ] Product Name / Product Number

(1-1) Product Name (Standard Form)

SG-8201CJ: X1G005981xxxx16

SG-8201CG: X1G006191xxxx16 (Please contact Epson for details)

(1-2) Product Number / Ordering Code

SG-8201CJ ① 25.000000MHz ③ T B H P A ④⑤⑥⑦⑧

①Model ②Size ③Frequency ④Supply voltage (T: 1.8 V to 3.3 V Typ.)

⑤Frequency tolerance ⑥Operating temperature ⑦Function ⑧Rise/Fall time

| ②Size | |
|---|---|
| CJ | 2.0 mm × 1.6 mm |
| CG | 2.5 mm × 2.0 mm |

| ⑤Frequency tolerance / ⑥Operating temperature | |
|---|---|
| BH | ±15 × $10^{-6}$ / -40 °C to +105 °C |
| DJ | ±25 × $10^{-6}$ / -40 °C to +125 °C |

| ⑦Function | |
|---|---|
| P | Output enable (#1pin = OE) |
| Q | Output enable (#1pin = $\overline{OE}$) |
| S | Standby (#1pin = $\overline{ST}$) |
| T | Standby (#1pin = ST) |

| ⑧Rise/Fall time | |
|---|---|
| A | Default |
| B | Faster |
| C | Fast |
| D | Slow |
| E | Slower |

[ 2 ] Absolute Maximum Ratings

| Parameter | Symbol | Specification | | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Maximum supply voltage | GND-$V_{CC}$ | -0.3 | - | 4 | V | GND = 0 V |
| Input voltage | $V_{IN}$ | GND - 0.3 | - | $V_{CC}$ + 0.3 | V | #1 pin |
| Storage temperature range | T_stg | -55 | - | +125 | °C | |

[ 3 ] Operating Range

| Parameter | Symbol | Specification | | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Supply voltage | $V_{CC}$ | 1.62 | - | 3.63 | V | |
| Supply voltage | GND | 0.0 | 0.0 | 0.0 | V | |
| Input voltage | $V_{IN}$ | GND | - | $V_{CC}$ | V | #1 pin |
| Operating temperature range | T_use | -40 | +25 | +105 | °C | |
| | | -40 | +25 | +125 | °C | |
| CMOS load condition | L_CMOS | - | - | 15 | pF | |

* Power supply startup time (0 %$V_{CC}$ → 90 %$V_{CC}$) should be between 5 µs and 500 ms

* A 0.01 µF to 0.1 µF or over bypass capacitor should be connected between $V_{CC}$ and GND pins located close to the device

[ 4 ] Frequency Characteristics (Unless stated otherwise [ 3 ] Operating Range)

| Parameter | Symbol | Specification | | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Output frequency | fo | 1.2 | | 170 | MHz | |
| | | -15 | - | +15 | ×$10^{-6}$ | T_use = -40 °C to +105 °C |
| | | -25 | - | +25 | ×$10^{-6}$ | T_use = -40 °C to +125 °C |
| Frequency aging *2 | f_age | Included in frequency tolerance | | | ×$10^{-6}$ | +25 °C, First year |

*1 Frequency tolerance includes initial frequency tolerance, frequency / temperature characteristics, frequency / voltage coefficient, frequency / load coefficient and frequency aging (+25 °C, first year)

*2 Frequency aging is estimated from environmental reliability tests; expected amount of the frequency variation. This is not intended to be a guarantee of the product life cycle.

[ 5 ] Electrical Characteristics (Unless stated otherwise [ 3 ] Operating Range)

| Parameter | Symbol | Specification | | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Start-up time | t_str | - | - | 3 | ms | t = 0 at $V_{CC}$ > 1.62 V |
| Current consumption (No load) $V_{CC}$ = 1.62 V to 1.98 V | $I_{CC}$ | - | 5.2 | 7.0 | mA | 1.2 MHz ≤ fo ≤ 25 MHz |
| | | - | 5.4 | 7.3 | | 25 MHz < fo ≤ 50 MHz |
| | | - | 5.7 | 7.7 | | 50 MHz < fo ≤ 75 MHz |
| | | - | 6.2 | 8.2 | | 75 MHz < fo ≤ 100 MHz |
| | | - | 6.9 | 9.4 | | 100 MHz < fo ≤ 125 MHz |
| | | - | 7.8 | 10.4 | | 125 MHz < fo ≤ 170 MHz |
| Current consumption (No load) $V_{CC}$ = 2.25 V to 2.75 V | | - | 5.4 | 7.2 | mA | 1.2 MHz ≤ fo ≤ 25 MHz |
| | | - | 5.7 | 7.6 | | 25 MHz < fo ≤ 50 MHz |
| | | - | 6.3 | 8.2 | | 50 MHz < fo ≤ 75 MHz |
| | | - | 6.9 | 9.1 | | 75 MHz < fo ≤ 100 MHz |
| | | - | 7.9 | 10.7 | | 100 MHz < fo ≤ 125 MHz |
| | | - | 9.2 | 12.4 | | 125 MHz < fo ≤ 170 MHz |
| Current consumption (No load) $V_{CC}$ = 2.97 V to 3.63 V | | - | 5.6 | 7.5 | mA | 1.2 MHz ≤ fo ≤ 25 MHz |
| | | - | 6.1 | 8.1 | | 25 MHz < fo ≤ 50 MHz |
| | | - | 7.0 | 9.1 | | 50 MHz < fo ≤ 75 MHz |
| | | - | 7.9 | 10.4 | | 75 MHz < fo ≤ 100 MHz |
| | | - | 9.1 | 12.4 | | 100 MHz < fo ≤ 125 MHz |
| | | - | 11.2 | 15.0 | | 125 MHz < fo ≤ 170 MHz |
| Disable current | I_dis | - | 5.0 | 7.2 | mA | $V_{CC}$ = 1.62 V to 1.98 V |
| | | - | 5.0 | 7.3 | | $V_{CC}$ = 2.25 V to 2.75 V |
| | | - | 5.1 | 7.4 | | $V_{CC}$ = 2.97 V to 3.63 V |
| Stand-by current | I_std | - | 0.3 | 15.0 | µA | $V_{CC}$ = 1.62 V to 1.98 V |
| | | - | 0.3 | 15.0 | | $V_{CC}$ = 2.25 V to 2.75 V |
| | | - | 0.5 | 15.0 | | $V_{CC}$ = 2.97 V to 3.63 V |
| Output voltage (DC characteristics) | $V_{OH}$ | 90 % $V_{CC}$ | - | - | V | Rise/Fall time: Default 'A' Option *1 / Other Options / $I_{OH}$ / $I_{OL}$<br>fo > 125 MHz / 'B' / -2.0 mA / 2.0 mA<br>75 MHz < fo ≤ 125 MHz / 'C' / -1.0 mA / 1.0 mA<br>50 MHz < fo ≤ 75 MHz / 'D' / -0.5 mA / 0.5 mA<br>fo ≤ 50 MHz / 'E' / -0.2 mA / 0.2 mA |
| | $V_{OL}$ | - | - | 10 % $V_{CC}$ | V | |
| Symmetry | SYM | 45 | 50 | 55 | % | 50 % $V_{CC}$ level, L_CMOS ≤ 15 pF |
| Rise/Fall time | tr/tf | | | | | Default 'A' Option *1 / Other Options / Conditions |
| | | - | - | 2.0 | ns | fo > 125 MHz / 'B' / 20 % - 80 % $V_{CC}$ level, L_CMOS = 15 pF |
| | | - | - | 2.5 | | 75 MHz < fo ≤ 125 MHz / 'C' |
| | | - | - | 4.0 | | 50 MHz < fo ≤ 75 MHz / 'D' |
| | | - | - | 6.0 | | fo ≤ 50 MHz / 'E' |
| Input voltage | $V_{IH}$ | 70 % $V_{CC}$ | - | - | V | #1 pin |
| | $V_{IL}$ | - | - | 30 % $V_{CC}$ | V | |
| Input capacitance | $C_{IN}$ | - | 3 | 5 | pF | #1 pin |
| Input pull up resistance (OE) | $R_{UP1}$ | - | 40 | - | kΩ | |
| Input pull up resistance ($\overline{ST}$) | $R_{UP1}$ | - | 40 | - | kΩ | $\overline{ST}$ = 70 % $V_{CC}$ |
| | $R_{UP2}$ | - | 10 | - | MΩ | $\overline{ST}$ = 30 % $V_{CC}$ |
| Input pull up resistance (ST) | $R_{UP1}$ | - | 40 | - | kΩ | |
| Input pull down resistance ($\overline{OE}$) | $R_{DN1}$ | - | 40 | - | kΩ | |
| Output pull down resistance | $R_{DN}$ | - | 500 | - | kΩ | |
| Output disable time (OE) | tstp_oe | - | - | 1 | µs | Measured from the time OE pin crosses 30 % $V_{CC}$ or measured from the time $\overline{OE}$ pin crosses 70 % $V_{CC}$ |
| Output disable time (ST) | tstp_st | - | - | 1 | µs | Measured from the time $\overline{ST}$ pin crosses 30 % $V_{CC}$ or measured from the time ST pin crosses 70 % $V_{CC}$ |
| Output enable time (OE) | tsta_oe | - | - | 100 ns + 2 clock cycles | - | Measured from the time OE pin crosses 70 % $V_{CC}$ or measured from the time $\overline{OE}$ pin crosses 30 % $V_{CC}$ |
| Output enable time (ST) | tsta_st | - | - | 3 | ms | Measured from the time $\overline{ST}$ pin crosses 70 % $V_{CC}$ or measured from the time ST pin crosses 30 % $V_{CC}$ |

*1 Default 'A' Rise/Fall time is dependent on programmed frequency

(Unless stated otherwise [ 3 ] Operating Range)

| Parameter | Symbol | Specification | | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Phase jitter | $t_{PJ}$ | - | 1.2 | - | ps | fo = 25 MHz,<br>Offset frequency: 12 kHz to 5 MHz |
| | | - | 1.2 | - | | fo = 50 MHz,<br>Offset frequency: 12 kHz to 20 MHz |
| | | - | 1.2 | - | | fo = 75 MHz,<br>Offset frequency: 12 kHz to 20 MHz |
| | | - | 1.2 | - | | fo = 100 MHz,<br>Offset frequency: 12 kHz to 20 MHz |
| | | - | 1.1 | - | | fo = 125 MHz,<br>Offset frequency: 12 kHz to 20 MHz |
| | | - | 1.4 | - | | fo = 150 MHz,<br>Offset frequency: 12 kHz to 20 MHz |
| | | - | 1.5 | - | | fo = 170 MHz,<br>Offset frequency: 12 kHz to 20 MHz |

[ 6 ] Thermal Resistance (For Reference Only)

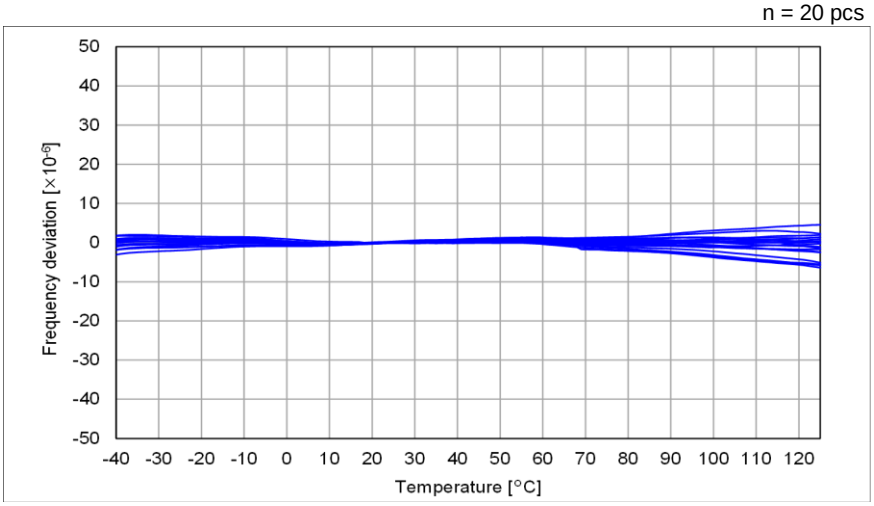
| Parameter | Symbol | Specification | | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Junction temperature | Tj | - | - | +150 | °C | |
| Junction to case | θjc | - | 129 | - | °C/W | SG-8201CJ |
| | | - | 121 | - | °C/W | SG-8201CG |
| Junction to ambient | θja | - | 257 | - | °C/W | SG-8201CJ |
| | | - | 208 | - | °C/W | SG-8201CG |

[ 7 ] Typical Performance Characteristics (For Reference Only)

The following data shows typical performance characteristics

(7-1) Frequency / Temperature Characteristics

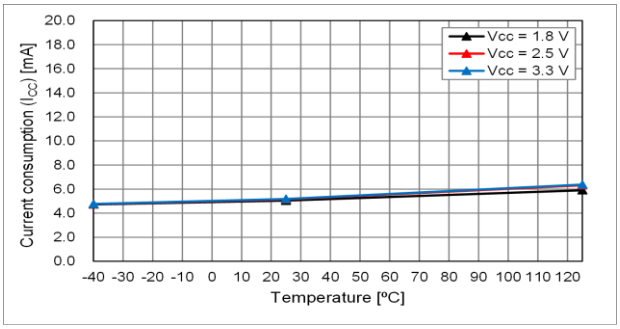
n = 20 pcs



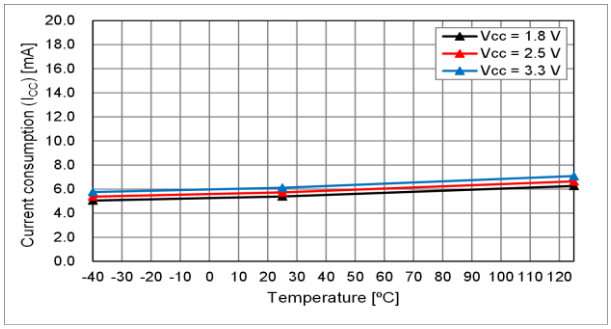
(7-2) Current Consumption

Temperature Characteristic (No load)

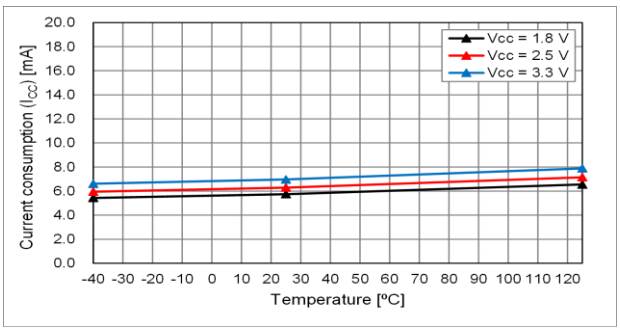
fo = 25 MHz



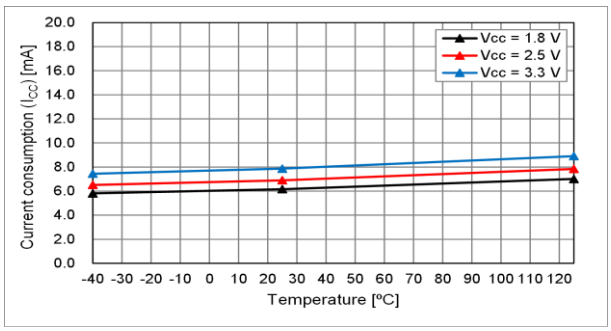

fo = 50 MHz



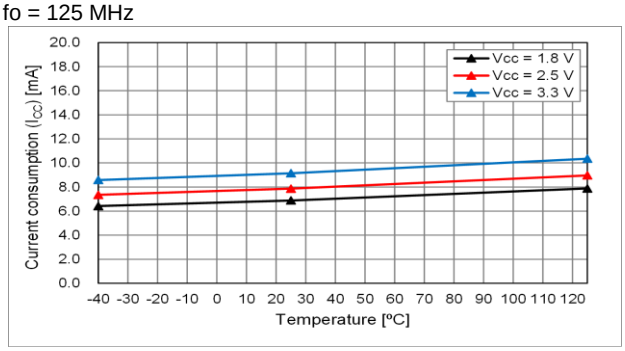

fo = 75 MHz



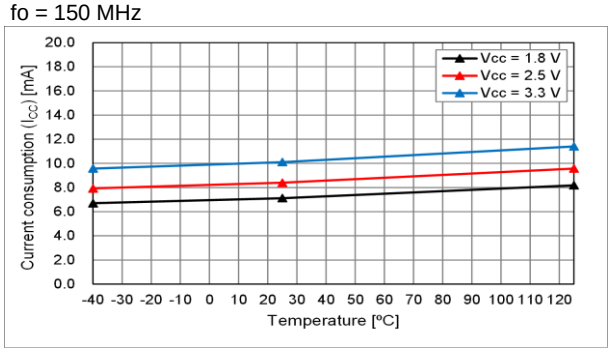

fo = 100 MHz



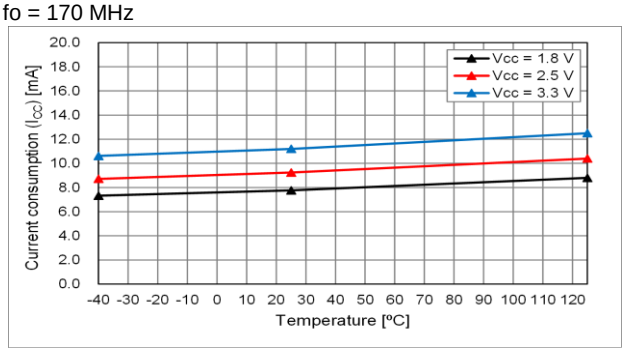

fo = 125 MHz




fo = 150 MHz



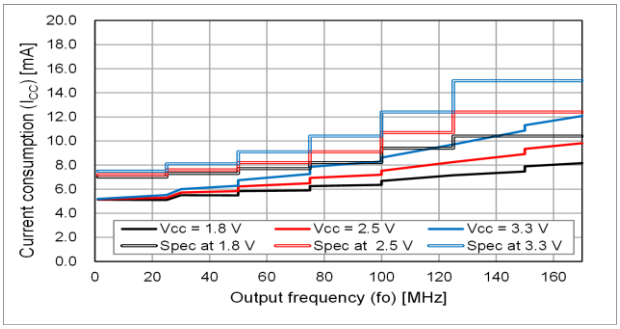

fo = 170 MHz



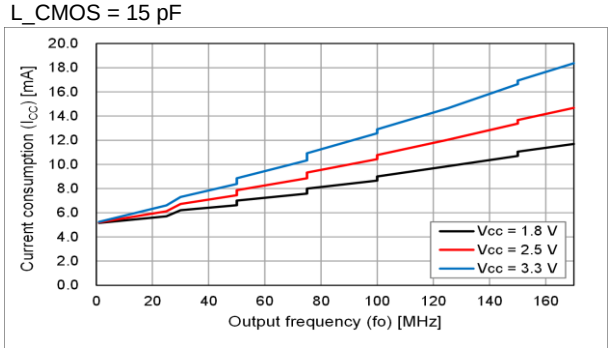
(7-2) Current Consumption [cont'd]

Frequency Dependency (T_use = +25 °C)

No load




L_CMOS = 15 pF

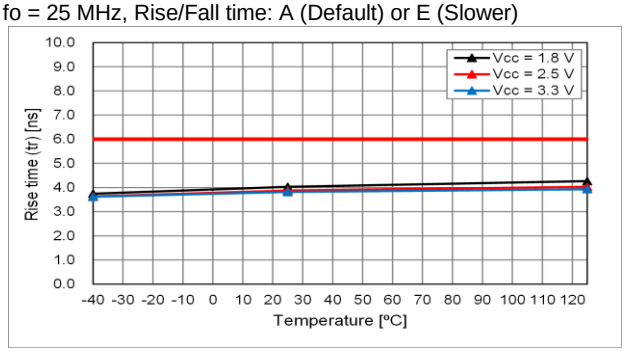


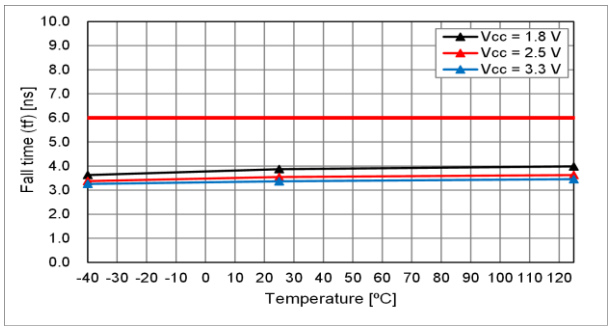

The actual current consumption is the total of the current under the condition of no load and the current to drive the output load (fo × L_CMOS × $V_{CC}$). To reduce the current consumption, it is effective to use lower frequency, lower supply voltage and lower output load.

(7-3) Rise/Fall Time

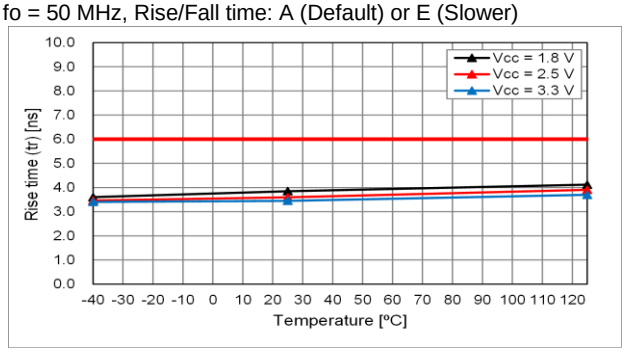
Temperature Characteristic (20 % - 80 %$V_{CC}$, L_CMOS = 15 pF)

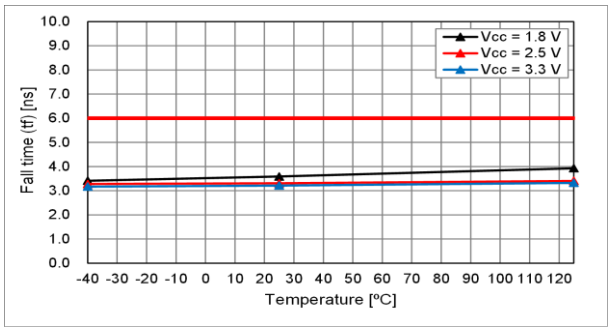
fo = 25 MHz, Rise/Fall time: A (Default) or E (Slower)



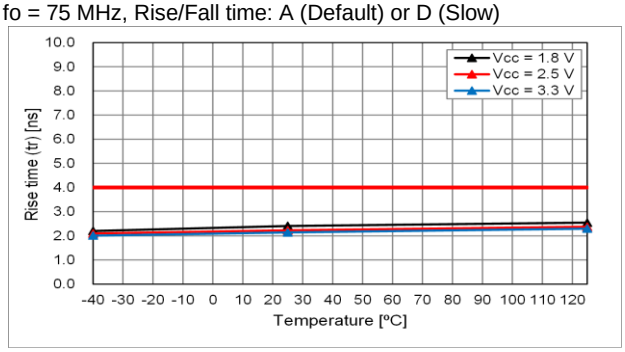



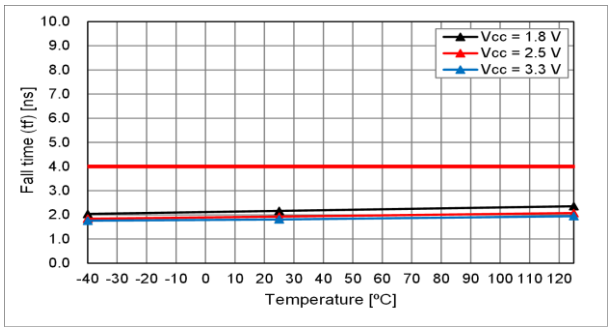

fo = 50 MHz, Rise/Fall time: A (Default) or E (Slower)




fo = 75 MHz, Rise/Fall time: A (Default) or D (Slow)

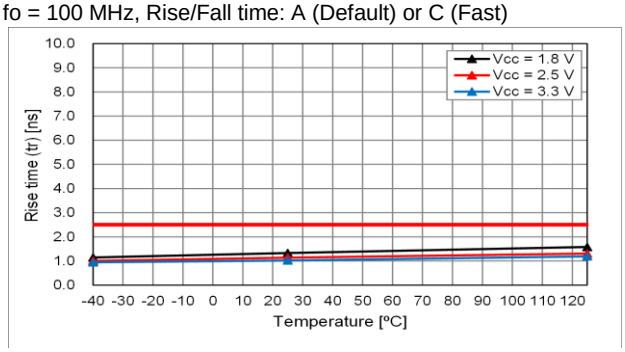


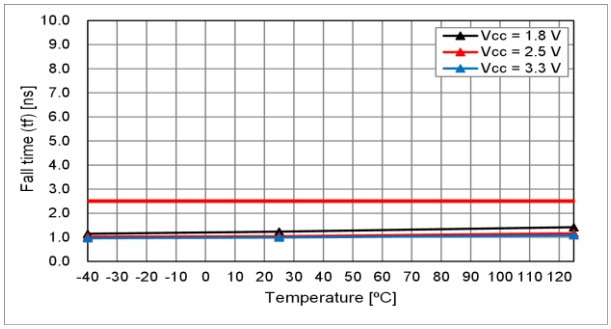



(7-3) Rise/Fall Time [cont'd]

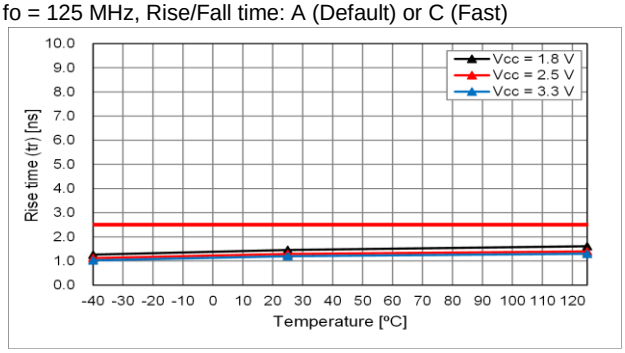
Temperature Characteristic (20 % - 80 %$V_{CC}$, L_CMOS = 15 pF)

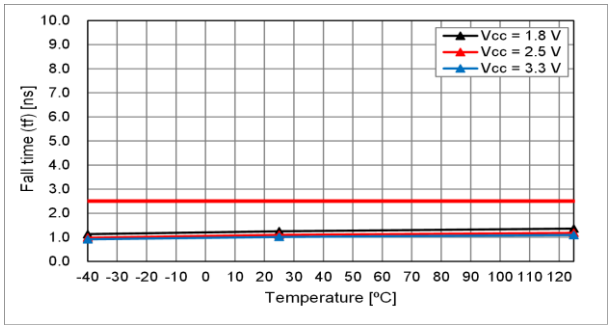
fo = 100 MHz, Rise/Fall time: A (Default) or C (Fast)



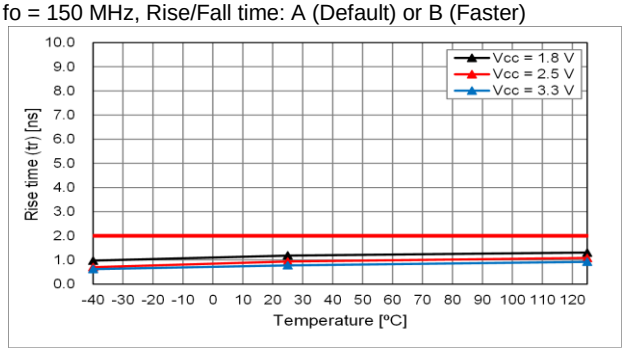



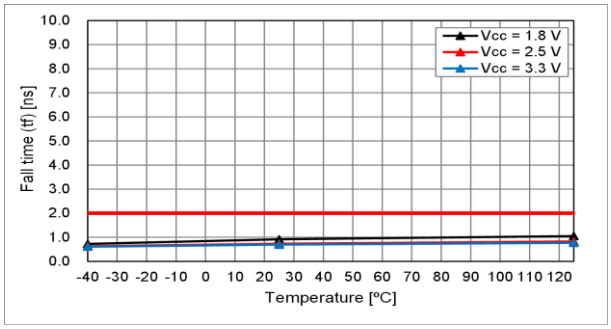

fo = 125 MHz, Rise/Fall time: A (Default) or C (Fast)



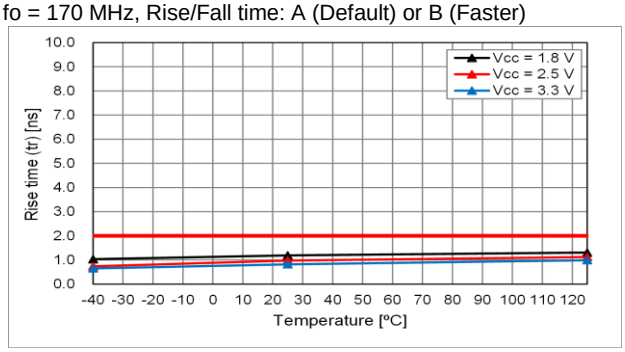



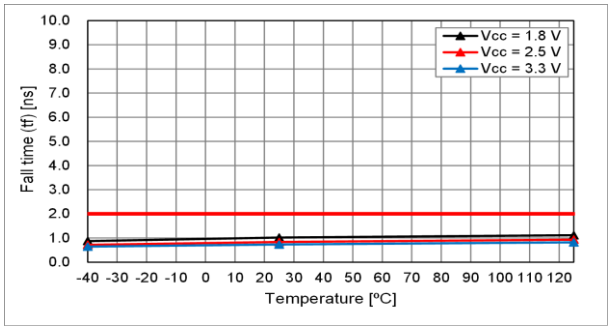

fo = 150 MHz, Rise/Fall time: A (Default) or B (Faster)




fo = 170 MHz, Rise/Fall time: A (Default) or B (Faster)

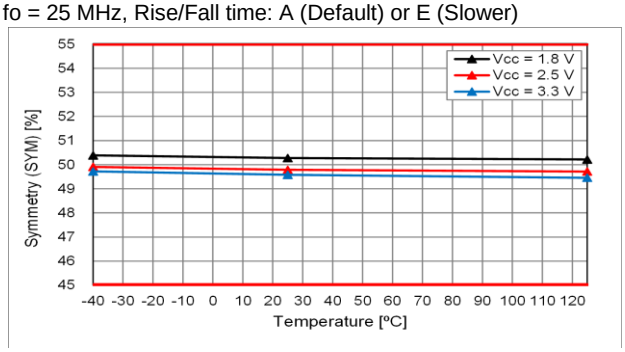


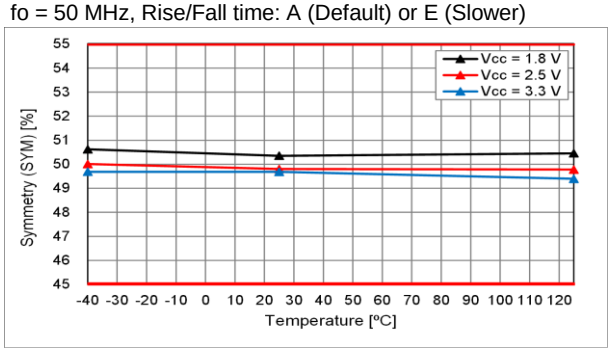
(7-4) Symmetry

Temperature Characteristic (L_CMOS = 15 pF)

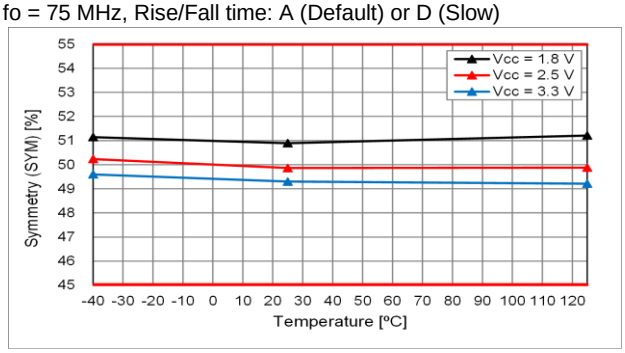
fo = 25 MHz, Rise/Fall time: A (Default) or E (Slower)



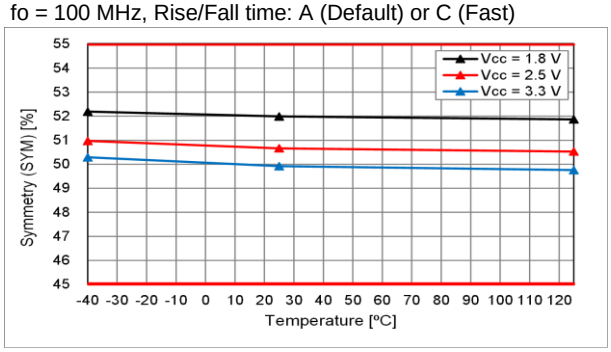

fo = 50 MHz, Rise/Fall time: A (Default) or E (Slower)



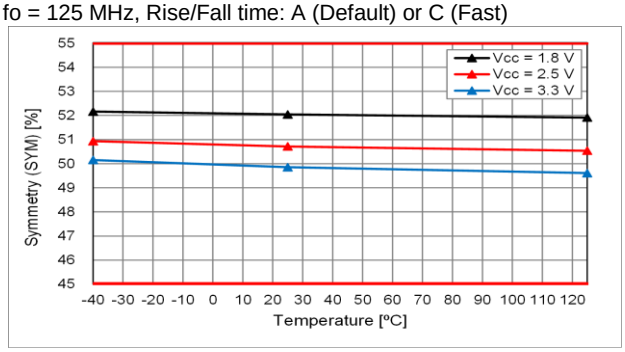

fo = 75 MHz, Rise/Fall time: A (Default) or D (Slow)



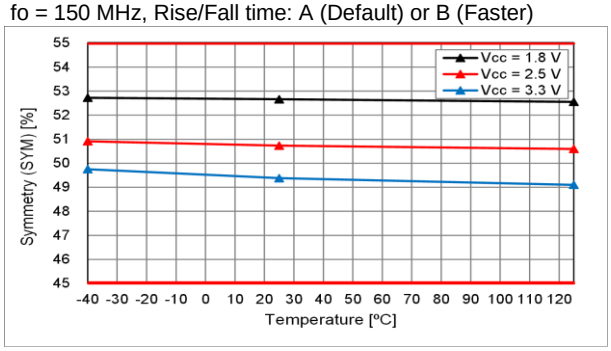

fo = 100 MHz, Rise/Fall time: A (Default) or C (Fast)



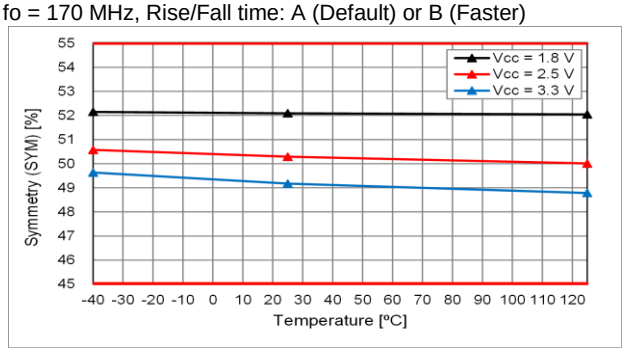

fo = 125 MHz, Rise/Fall time: A (Default) or C (Fast)




fo = 150 MHz, Rise/Fall time: A (Default) or B (Faster)



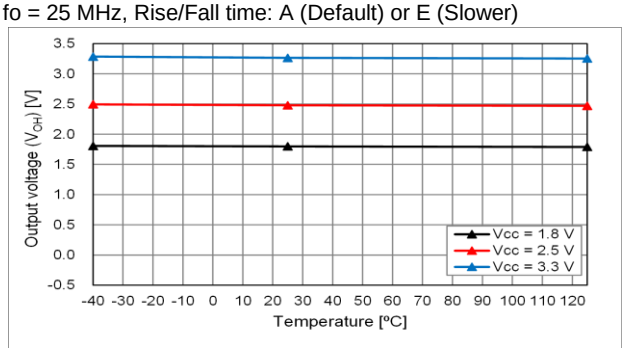

fo = 170 MHz, Rise/Fall time: A (Default) or B (Faster)

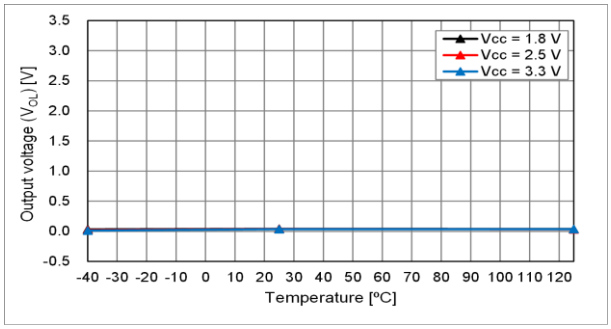


(7-5) Output Voltage

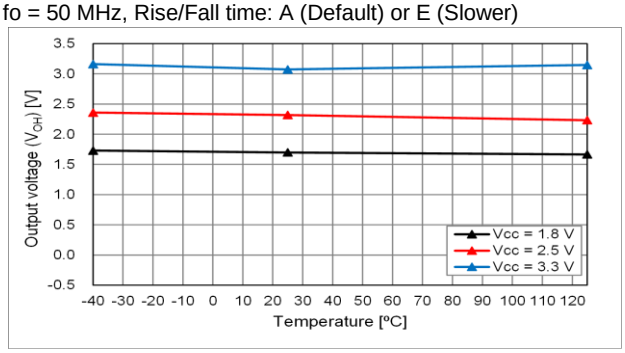
Temperature Characteristic (L_CMOS = 15 pF)

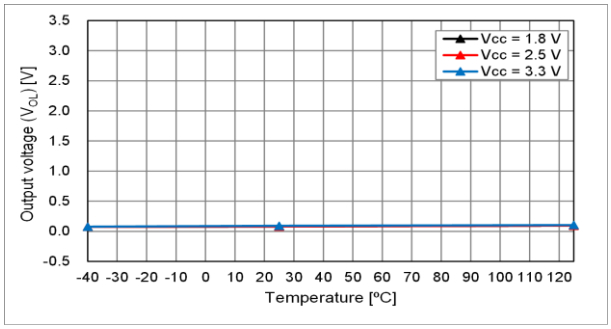
fo = 25 MHz, Rise/Fall time: A (Default) or E (Slower)



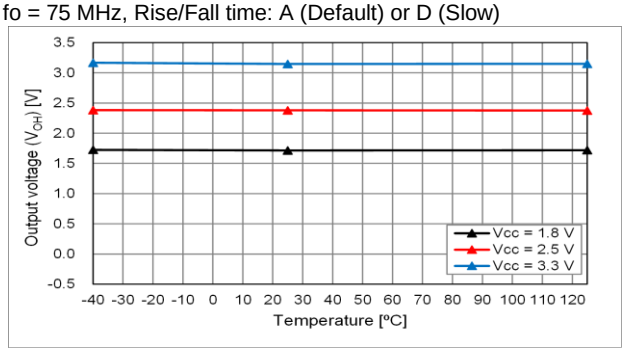



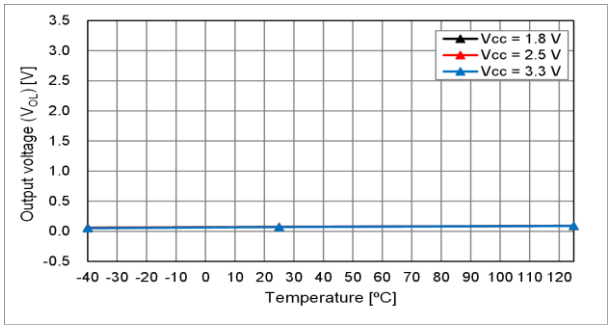

fo = 50 MHz, Rise/Fall time: A (Default) or E (Slower)



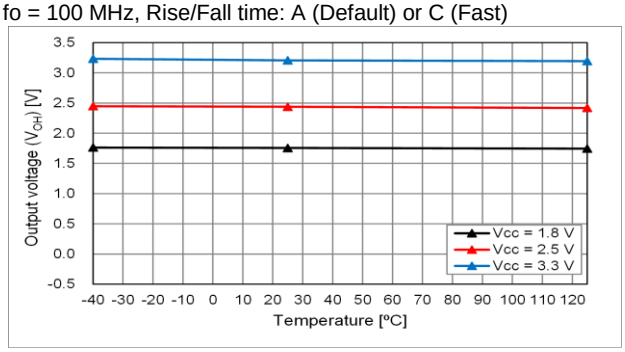



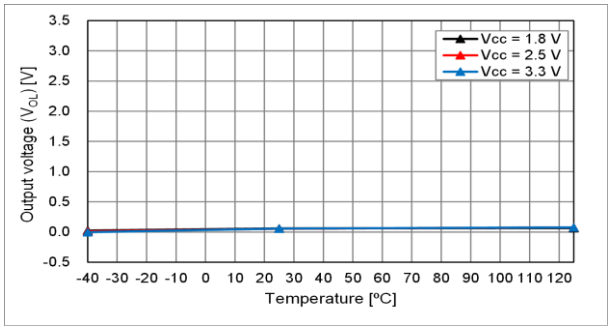

fo = 75 MHz, Rise/Fall time: A (Default) or D (Slow)




fo = 100 MHz, Rise/Fall time: A (Default) or C (Fast)

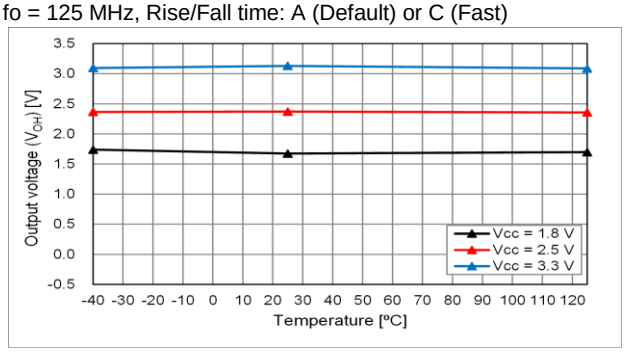


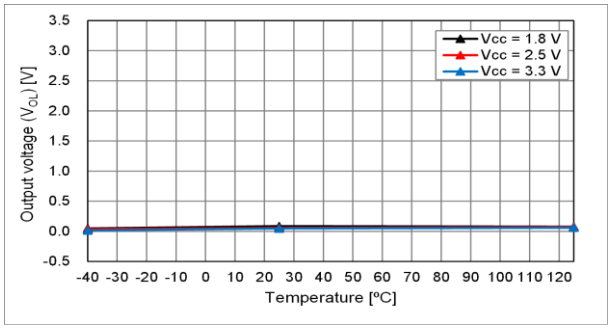



(7-5) Output Voltage [cont'd]

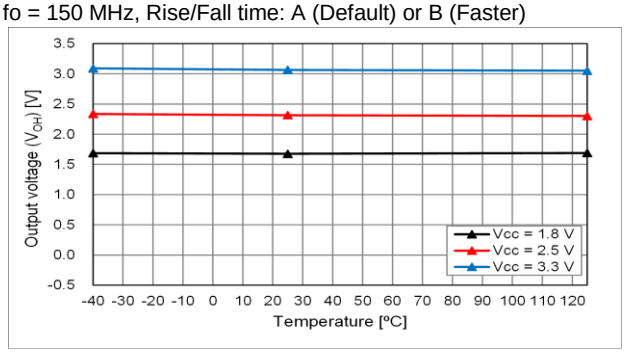
Temperature Characteristic (L_CMOS = 15 pF)

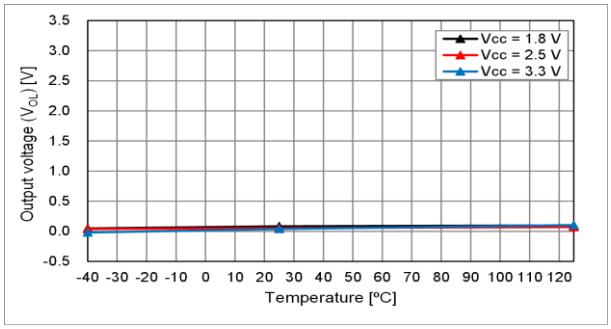
fo = 125 MHz, Rise/Fall time: A (Default) or C (Fast)



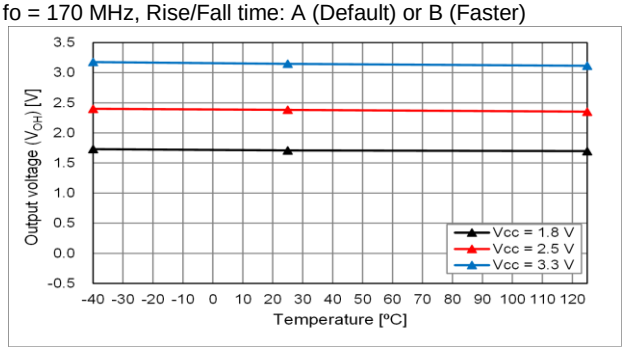



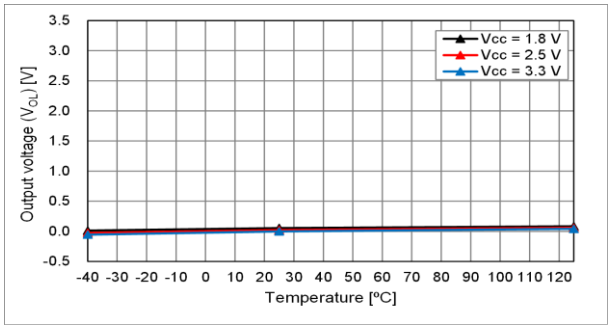

fo = 150 MHz, Rise/Fall time: A (Default) or B (Faster)




fo = 170 MHz, Rise/Fall time: A (Default) or B (Faster)

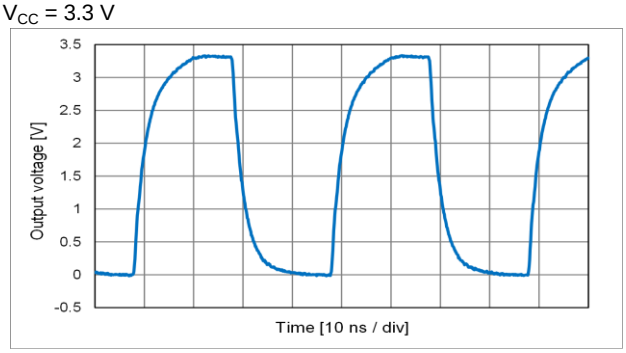


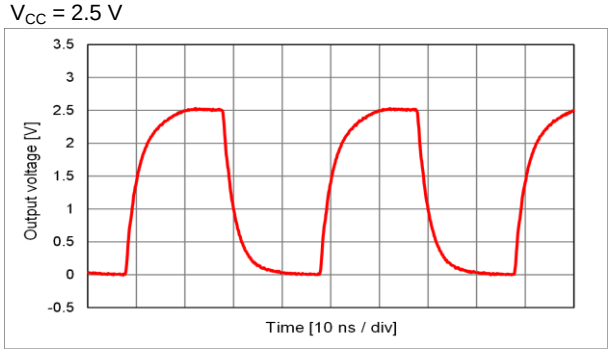
(7-6) Output Waveform

fo = 25 MHz, L_CMOS = 15 pF, T_use = +25 °C, Rise/Fall time: A (Default) or E (Slower)

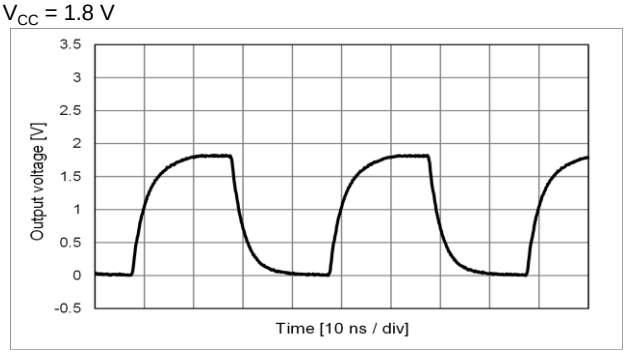
$V_{CC}$ = 3.3 V




$V_{CC}$ = 2.5 V

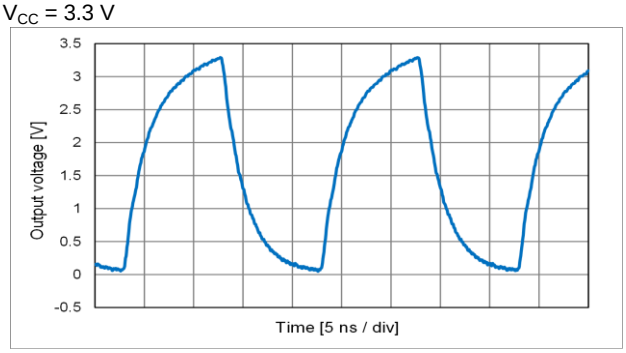



$V_{CC}$ = 1.8 V

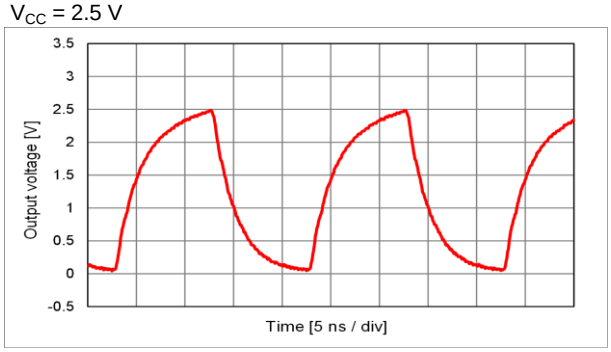



fo = 50 MHz, L_CMOS = 15 pF, T_use = +25 °C, Rise/Fall time: A (Default) or E (Slower)

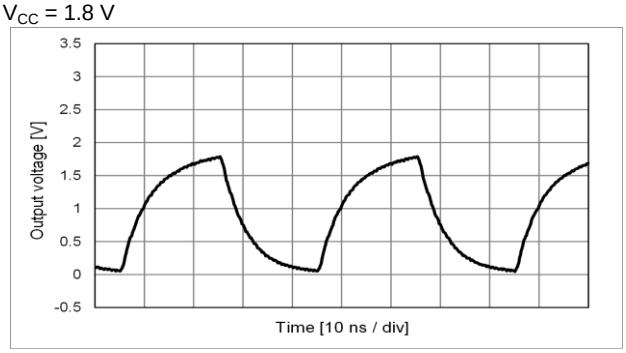
$V_{CC}$ = 3.3 V




$V_{CC}$ = 2.5 V



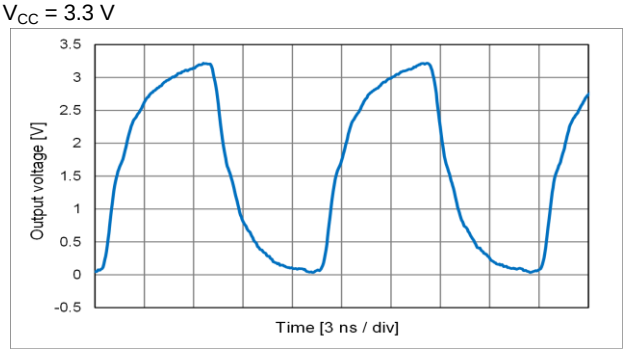

$V_{CC}$ = 1.8 V



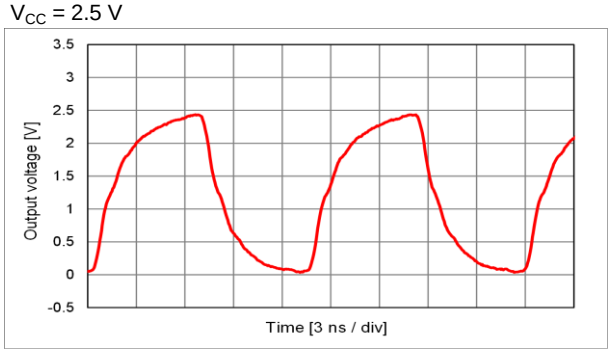
(7-6) Output Waveform [cont'd]

fo = 75 MHz, L_CMOS = 15 pF, T_use = +25 °C, Rise/Fall time: A (Default) or D (Slow)

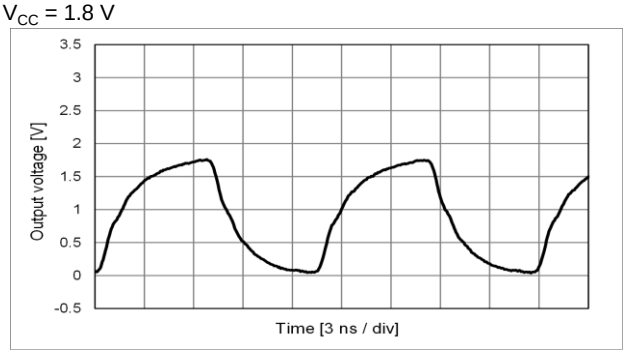
$V_{CC}$ = 3.3 V




$V_{CC}$ = 2.5 V

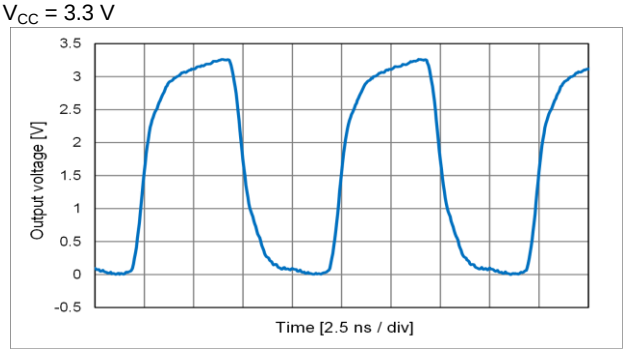



$V_{CC}$ = 1.8 V

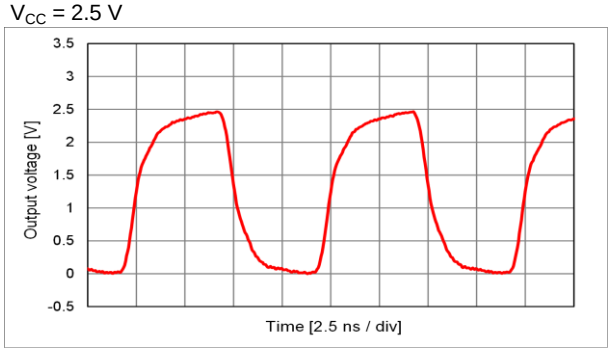



fo = 100 MHz, L_CMOS = 15 pF, T_use = +25 °C, Rise/Fall time: A (Default) or C (Fast)

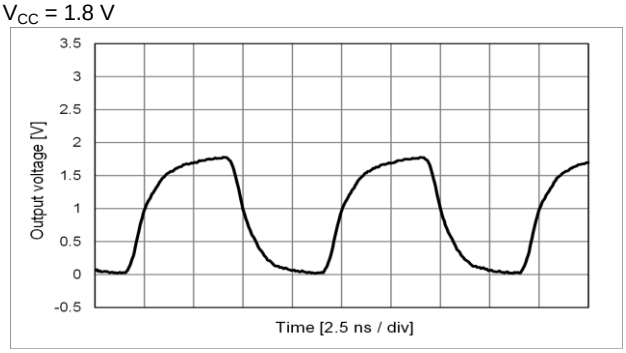
$V_{CC}$ = 3.3 V




$V_{CC}$ = 2.5 V



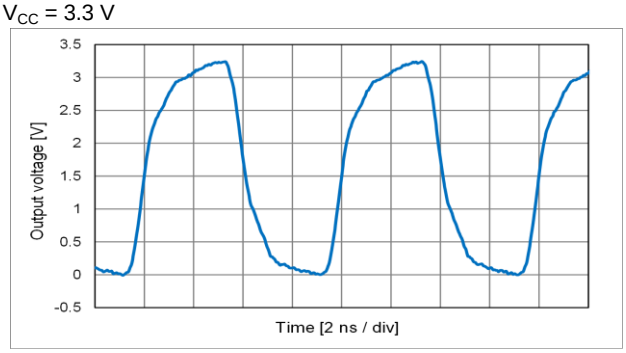

$V_{CC}$ = 1.8 V



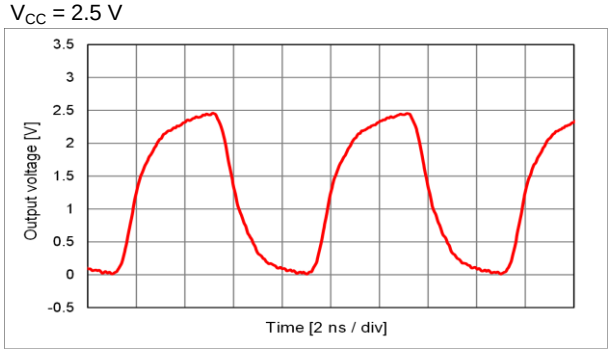
(7-6) Output Waveform [cont'd]

fo = 125 MHz, L_CMOS = 15 pF, T_use = +25 °C, Rise/Fall time: A (Default) or C (Fast)

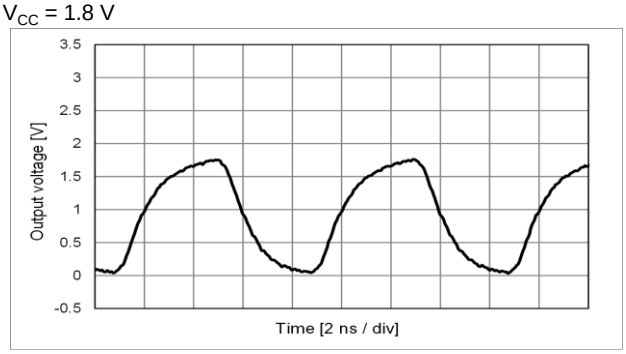
$V_{CC}$ = 3.3 V




$V_{CC}$ = 2.5 V

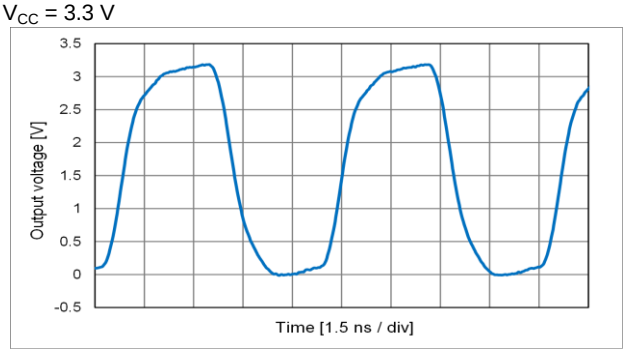



$V_{CC}$ = 1.8 V

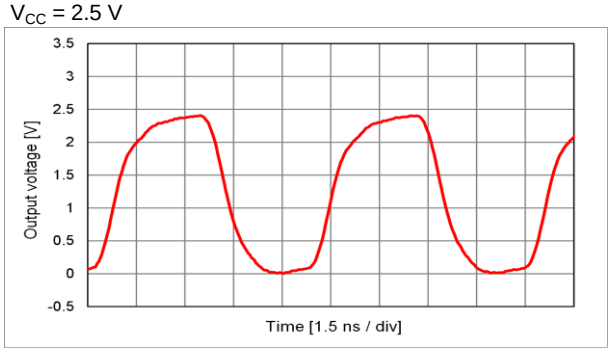



fo = 150 MHz, L_CMOS = 15 pF, T_use = +25 °C, Rise/Fall time: A (Default) or B (Faster)

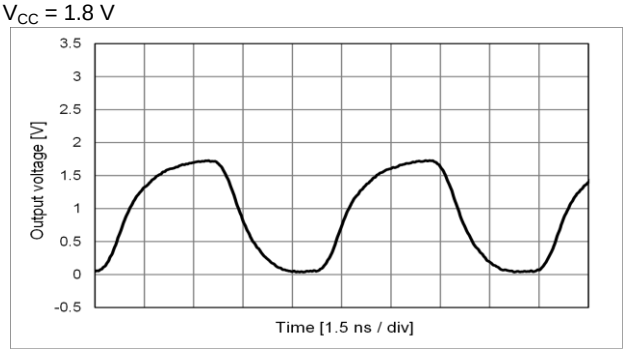
$V_{CC}$ = 3.3 V




$V_{CC}$ = 2.5 V



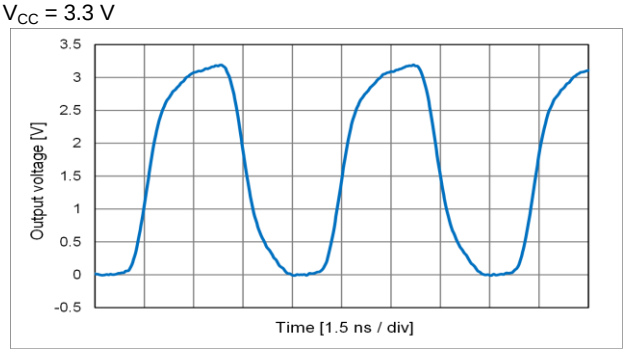

$V_{CC}$ = 1.8 V



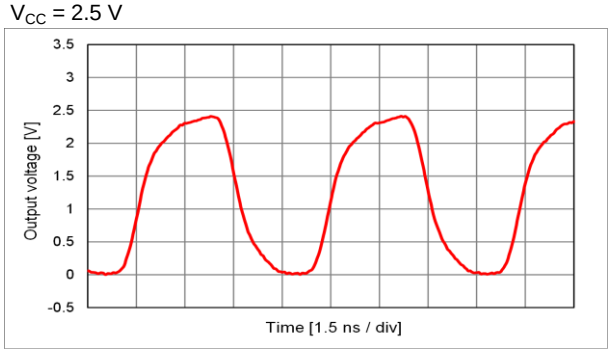
(7-6) Output Waveform [cont'd]

fo = 170 MHz, L_CMOS = 15 pF, T_use = +25 °C, Rise/Fall time: A (Default) or B (Faster)

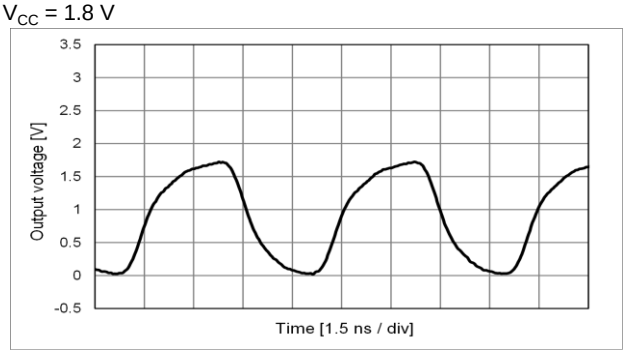
$V_{CC}$ = 3.3 V




$V_{CC}$ = 2.5 V

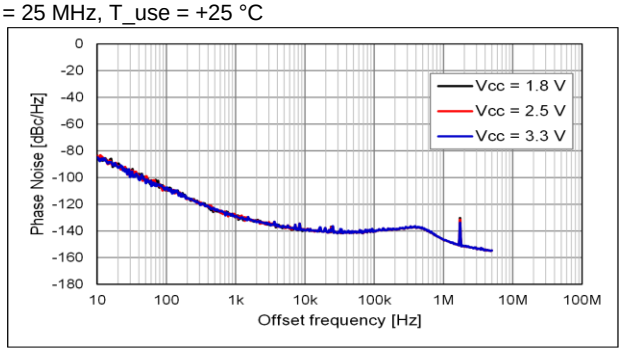



$V_{CC}$ = 1.8 V



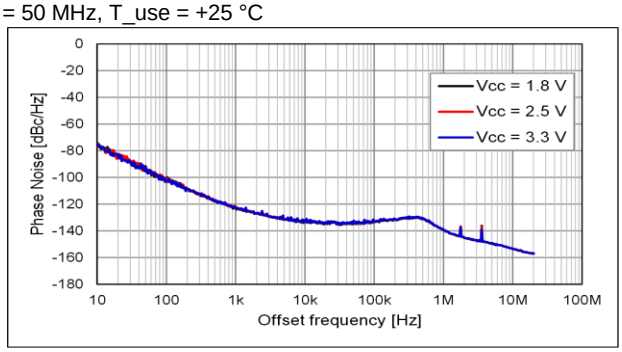
(7-7) Phase Noise and Phase Jitter

fo = 25 MHz, T_use = +25 °C



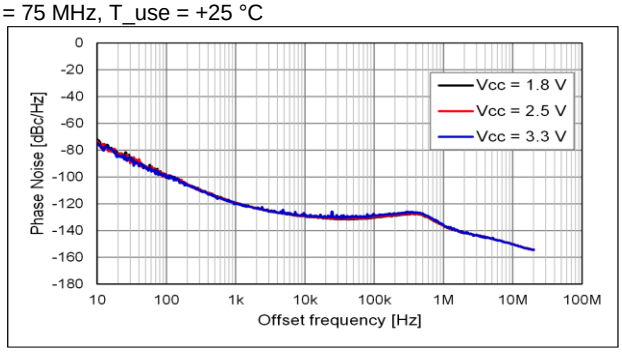

Phase jitter: 1.2 ps Typ.
Offset frequency: 12 kHz to 5 MHz

fo = 50 MHz, T_use = +25 °C



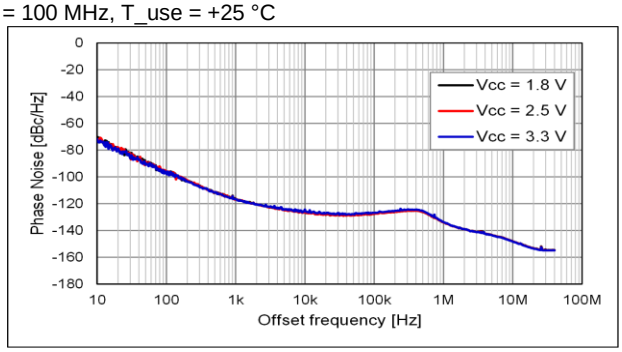

Phase jitter: 1.2 ps Typ.
Offset frequency: 12 kHz to 20 MHz

fo = 75 MHz, T_use = +25 °C




Phase jitter: 1.2 ps Typ.
Offset frequency: 12 kHz to 20 MHz

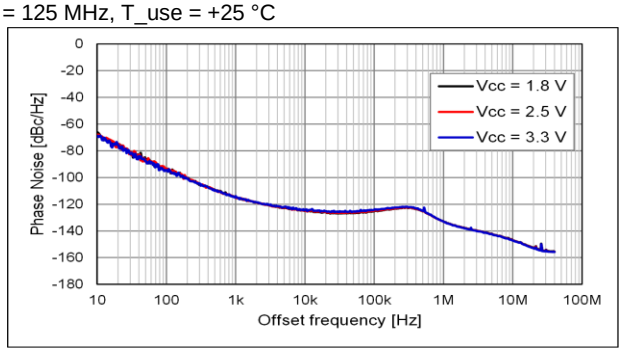
fo = 100 MHz, T_use = +25 °C




Phase jitter: 1.2 ps Typ.
Offset frequency: 12 kHz to 20 MHz

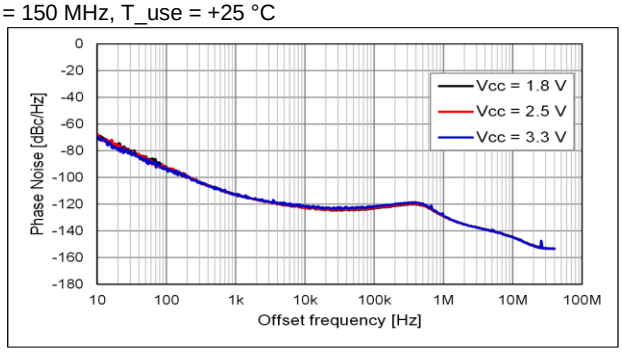
(7-7) Phase Noise and Phase Jitter [cont'd]

fo = 125 MHz, T_use = +25 °C



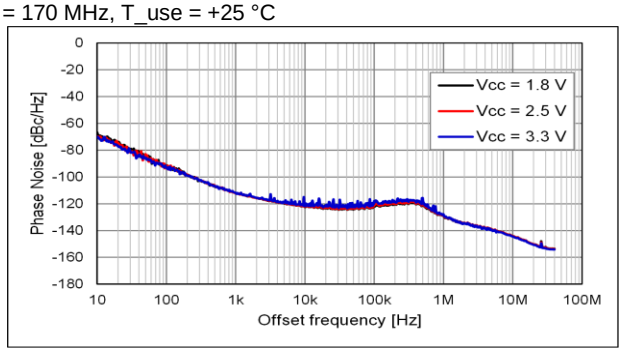

Phase jitter: 1.1 ps Typ.
Offset frequency: 12 kHz to 20 MHz

fo = 150 MHz, T_use = +25 °C




Phase jitter: 1.4 ps Typ.
Offset frequency: 12 kHz to 20 MHz

fo = 170 MHz, T_use = +25 °C

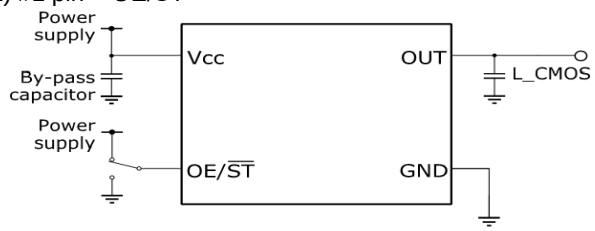



Phase jitter: 1.5 ps Typ.
Offset frequency: 12 kHz to 20 MHz

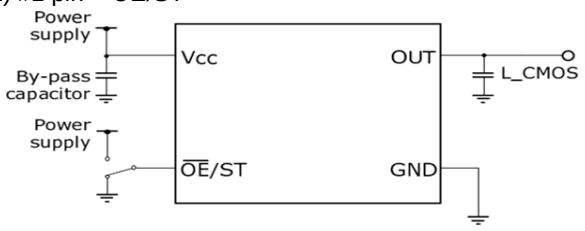
[ 8 ] Test Circuit

(8-1) Waveform Observation

(1) #1 pin = OE/$\overline{ST}$

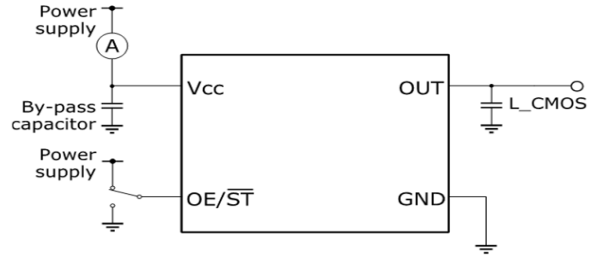



(2) #1 pin = $\overline{OE}$/ST



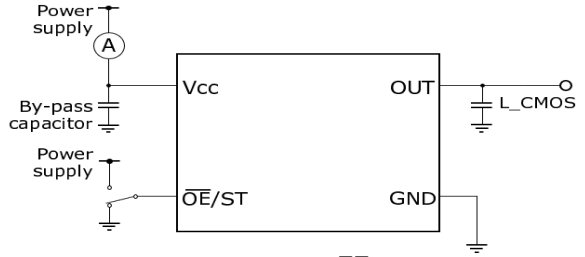

(8-2) Current Consumption Test

(1) #1 pin = OE/$\overline{ST}$




* Disable current test should be OE = GND.
Stand-by current test should be $\overline{ST}$ = GND.

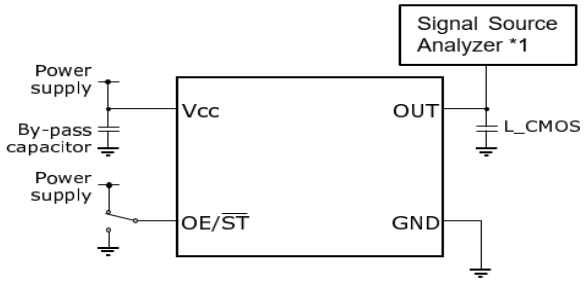
(2) #1 pin = $\overline{OE}$/ST



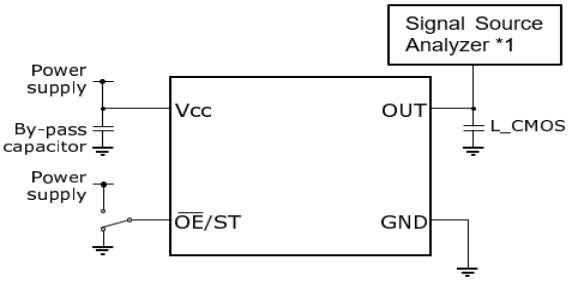

* Disable current test should be $\overline{OE}$ = $V_{CC}$.
Stand-by current test should be ST = $V_{CC}$.

(8-3) Jitter (Peak to Peak, RMS, Cycle to Cycle)

(1) #1 pin = OE/$\overline{ST}$




(2) #1 pin = $\overline{OE}$/ST




*1 Signal Source Analyzer: Keysight: E5052B, Minimum frequency = 10 MHz

(8-4) Condition

(1) Oscilloscope
The bandwidth should be minimum 5 times wider than measurement frequency
The probe ground should be placed closely to the test point and the lead length should be as short as possible
* It is recommended to use miniature socket. (Don't use earth lead.)

(2) L_CMOS includes probe capacitance.

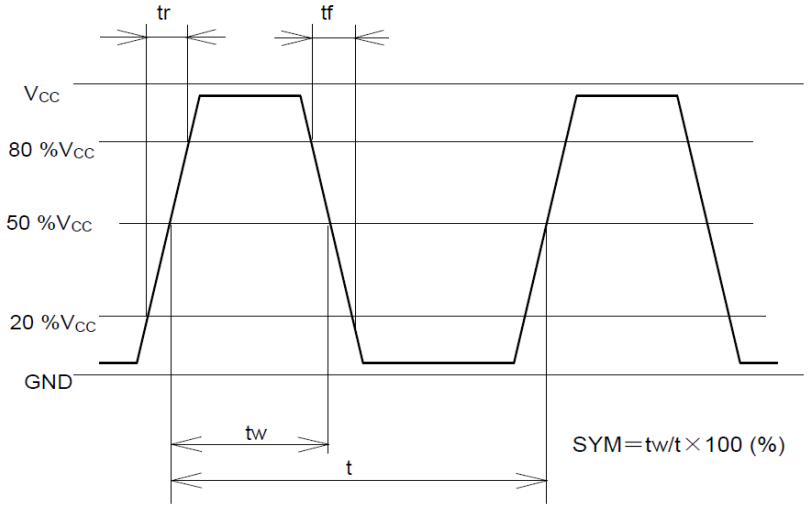
(3) A 0.01 µF to 0.1 µF bypass capacitor should be connected between $V_{CC}$ and GND pins located close to the device

(4) Use a current meter with a low internal impedance

(5) Power Supply
Power supply startup time (0 %$V_{CC}$ → 90 %$V_{CC}$) should be between 5 µs and 500 ms
Power supply impedance should be as low as possible and GND line should be as short as possible

[ 9 ] Timing Chart

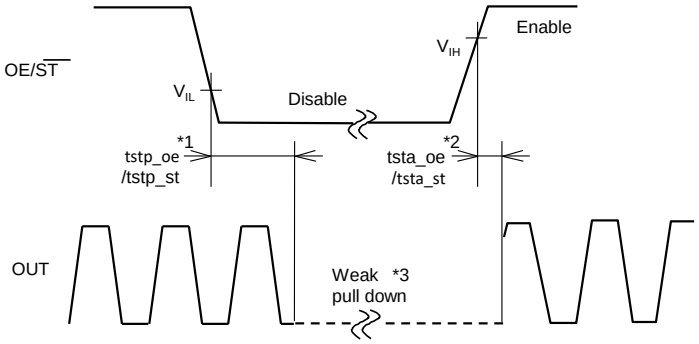
(9-1) Output Waveform and Level




(9-2) OE/$\overline{ST}$ Function and Timing

| OE terminal | Osc. circuit | Output status |
|---|---|---|
| High or Open | Oscillation | Specified frequency: Enable |
| Low | Oscillation | Low (Weak pull down*3): Disable |

| $\overline{ST}$ terminal | Osc. circuit | Output status |
|---|---|---|
| High | Oscillation | Specified frequency: Enable |
| Low | Oscillation stop | Low (Weak pull down*3): Disable |




*1 The period from OE/$\overline{ST}$ = $V_{IL}$ to OUT = Disable (Low, weak pull down)

*2 The period from OE/$\overline{ST}$ = $V_{IH}$ to OUT = Enable

*3 Pulled down with Output pull down resistance ($R_{DN}$)

* Judging the start of output when output waveform is observed.

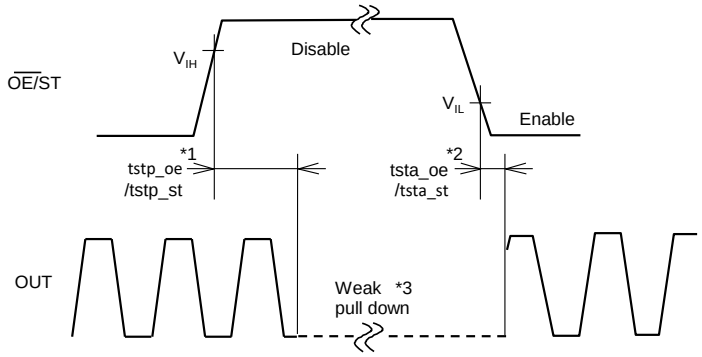
* OE/$\overline{ST}$ terminal voltage level should not exceed supply voltage when using OE/$\overline{ST}$ function.
  Please note that OE/$\overline{ST}$ rise time should not exceed supply voltage rise time at the start-up.

* Please do not use the $\overline{ST}$ terminal with the open state.
  If output should be enabled with the open state, please use Output Enable function.

(9-3) $\overline{OE}$/ST Function and Timing

| $\overline{OE}$ terminal | Osc. circuit | Output status |
|---|---|---|
| Low or Open | Oscillation | Specified frequency: Enable |
| High | Oscillation | Low (Weak pull down*3): Disable |

| ST terminal | Osc. circuit | Output status |
|---|---|---|
| Low | Oscillation | Specified frequency: Enable |
| High | Oscillation stop | Low (Weak pull down*3): Disable |




*1 The period from $\overline{OE}$/ST = $V_{IH}$ to OUT = Disable (Low, weak pull down)

*2 The period from $\overline{OE}$/ST = $V_{IL}$ to OUT = Enable

*3 Pulled down with Output pull down resistance ($R_{DN}$)

* Judging the start of output when output waveform is observed.

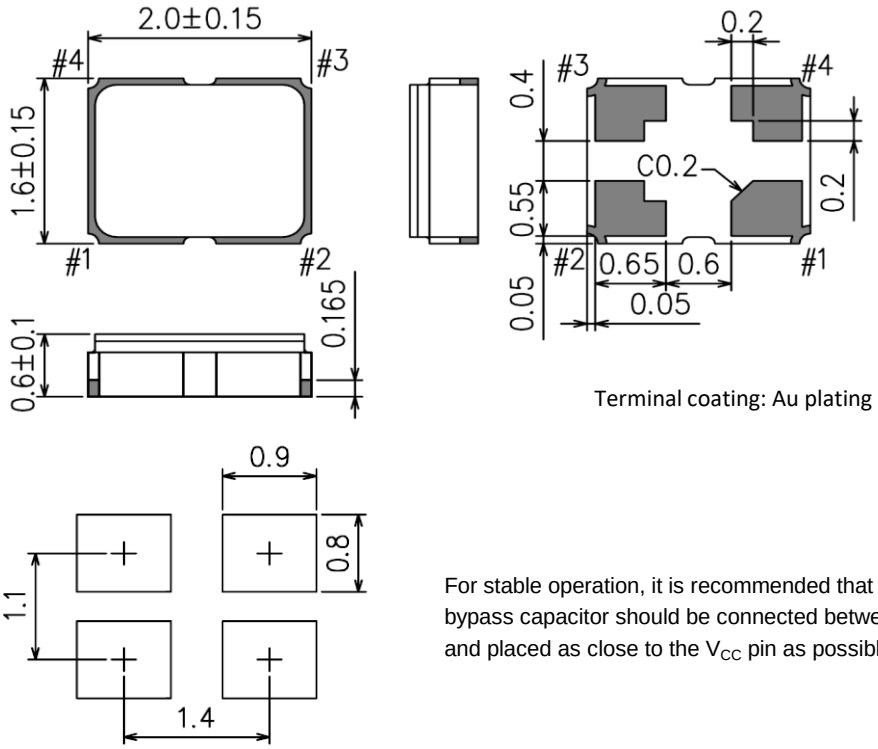
* $\overline{OE}$/ST terminal voltage level should not exceed supply voltage when using $\overline{OE}$/ST function.

* Please do not use the ST terminal with the open state.
  If output should be enabled with the open state, please use Output Enable function.

[ 10 ] Outline Drawing and Recommended Footprint

(10-1) SG-8201CJ

Units: mm




Terminal coating: Au plating




For stable operation, it is recommended that 0.01 µF to 0.1 µF bypass capacitor should be connected between $V_{CC}$ and GND and placed as close to the $V_{CC}$ pin as possible.

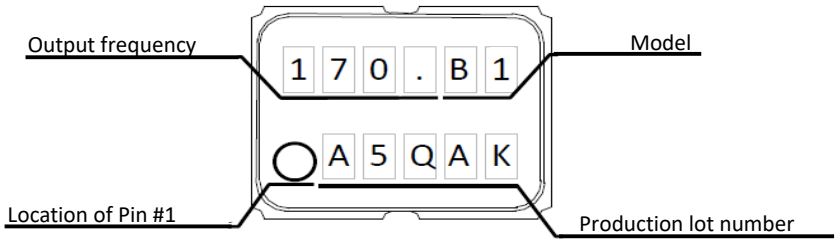
Reference Weight Typ.: 7.3 mg

Terminal Assignment

| Pin # | Name | Function | | |
|---|---|---|---|---|
| #1 | OE | Output Enable | High[*1] or Open: | Specified frequency output from OUT pin |
| | | | Low: | OUT pin is low (pull down with 500 kΩ), only output driver is disabled |
| | $\overline{OE}$ | Output Enable | Low[*2] or Open: | Specified frequency output from OUT pin |
| | | | High: | OUT pin is low (pull down with 500 kΩ), only output driver is disabled |
| | $\overline{ST}$ | Standby | High[*1 *3]: | Specified frequency output from OUT pin |
| | | | Low: | OUT pin is low (pull down with 500 kΩ)<br>Device goes to standby mode. Supply current reduces to the least as I_std |
| | ST | Standby | Low[*2 *3]: | Specified frequency output from OUT pin |
| | | | High: | OUT pin is low (pull down with 500 kΩ)<br>Device goes to standby mode. Supply current reduces to the least as I_std |
| #2 | GND | Ground | | |
| #3 | OUT | Clock output | | |
| #4 | $V_{CC}$ | Power supply | | |

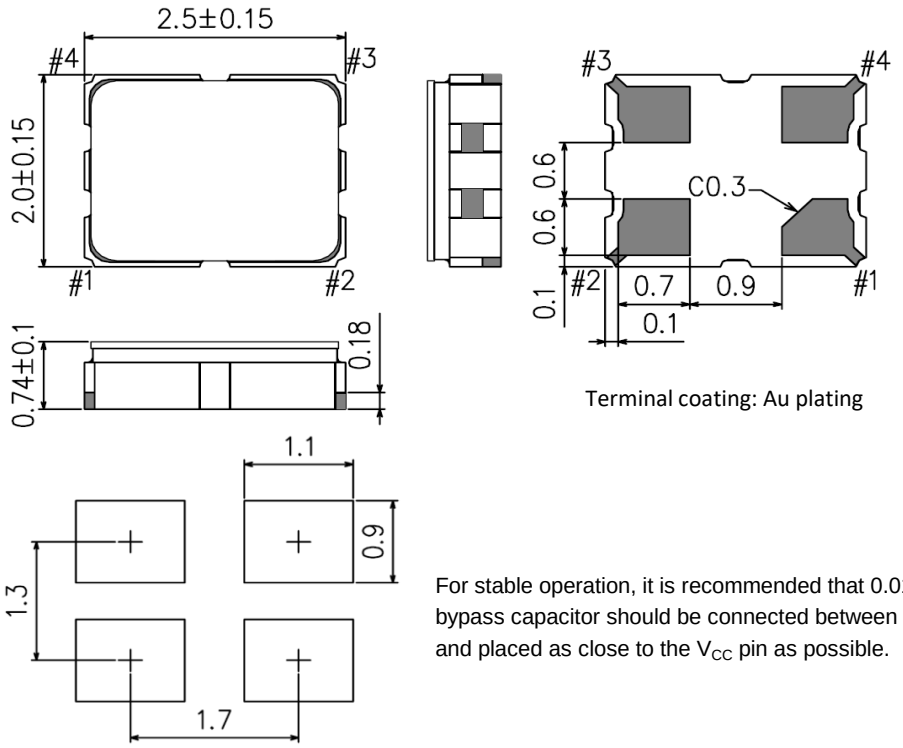
*1 If fixing it at High, please connect to $V_{CC}$ directly.
*2 If fixing it at Low , please connect to GND directly.
*3 If necessary to use Open, please select Output Enable function.

Marking



(10-2) SG-8201CG

Units: mm




For stable operation, it is recommended that 0.01 µF to 0.1 µF bypass capacitor should be connected between $V_{CC}$ and GND and placed as close to the $V_{CC}$ pin as possible.

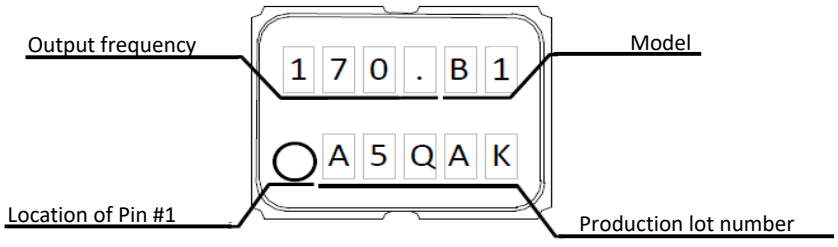
Reference Weight Typ.: 12 mg

Terminal Assignment

| Pin # | Name | Function | | |
|---|---|---|---|---|
| #1 | OE | Output Enable | High[*1] or Open: | Specified frequency output from OUT pin |
| | | | Low: | OUT pin is low (pull down with 500 kΩ), only output driver is disabled |
| | $\overline{OE}$ | Output Enable | Low[*2] or Open: | Specified frequency output from OUT pin |
| | | | High: | OUT pin is low (pull down with 500 kΩ), only output driver is disabled |
| | $\overline{ST}$ | Standby | High[*1 *3]: | Specified frequency output from OUT pin |
| | | | Low: | OUT pin is low (pull down with 500 kΩ)<br>Device goes to standby mode. Supply current reduces to the least as I_std |
| | ST | Standby | Low[*2 *3]: | Specified frequency output from OUT pin |
| | | | High: | OUT pin is low (pull down with 500 kΩ)<br>Device goes to standby mode. Supply current reduces to the least as I_std |
| #2 | GND | Ground | | |
| #3 | OUT | Clock output | | |
| #4 | $V_{CC}$ | Power supply | | |

*1 If fixing it at High, please connect to $V_{CC}$ directly.
*2 If fixing it at Low , please connect to GND directly.
*3 If necessary to use Open, please select Output Enable function.

Marking

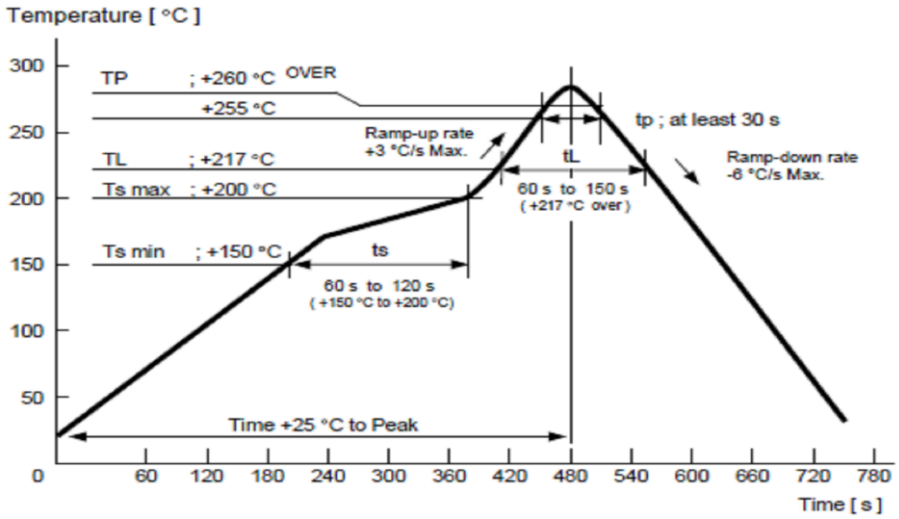


[ 11 ] Moisture Sensitivity Level

| Parameter | Specification | Conditions |
|---|---|---|
| MSL | LEVEL 1 | IPC/JEDEC J-STD-020D.1 |

[ 12 ] Reflow Profiles

IPC/JEDEC J-STD-020D.1



[ 13 ] Packing Information

(13-1) SG-8201CJ

(1) Packing Quantity

The last two digits of the Product Number (X1G005981xxxx**xx**) are a code that defines the packing quantity. The standard is "16" for a 3 000 pcs/Reel.

(2) Taping Specification

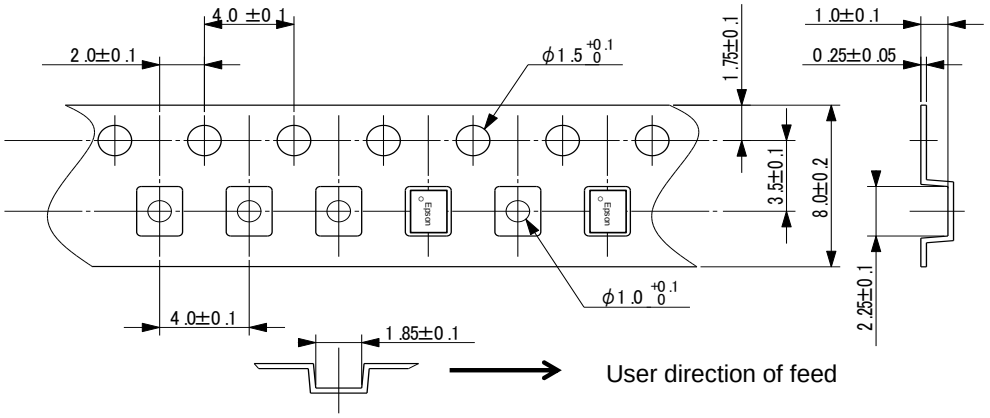
Subject to EIA-481, IEC-60286 and JIS C0806

1) Tape Dimensions

Carrier Tape Material: PS (Polystyrene)

Top Tape Material: PET (Polyethylene Terephthalate) + PE (Polyethylene)

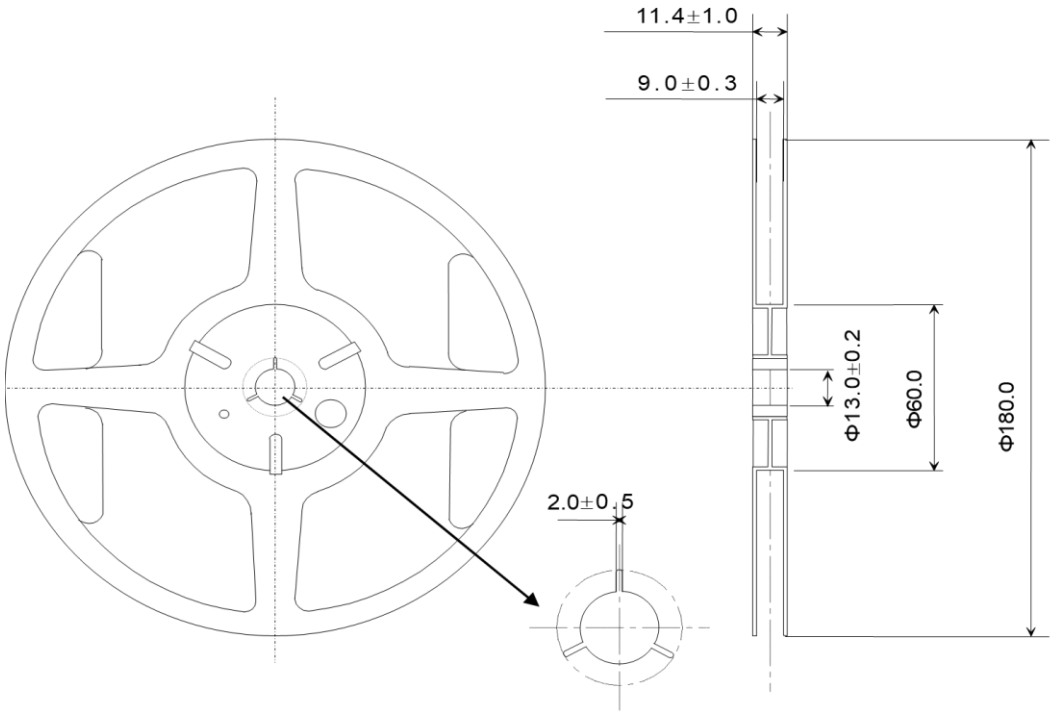
Units: mm




2) Reel Dimensions

Reel Material: PS (Polystyrene)

Units: mm




3) Storage Environment

We recommend to keep less than +30 °C and 85 %RH of humidity in a packed condition, and to use it less than 6 months after delivery.

(13-2) SG-8201CG

(1) Packing Quantity

The last two digits of the Product Number (X1G006191xxxx**xx**) are a code that defines the packing quantity. The standard is "16" for a 3 000 pcs/Reel.

(2) Taping Specification

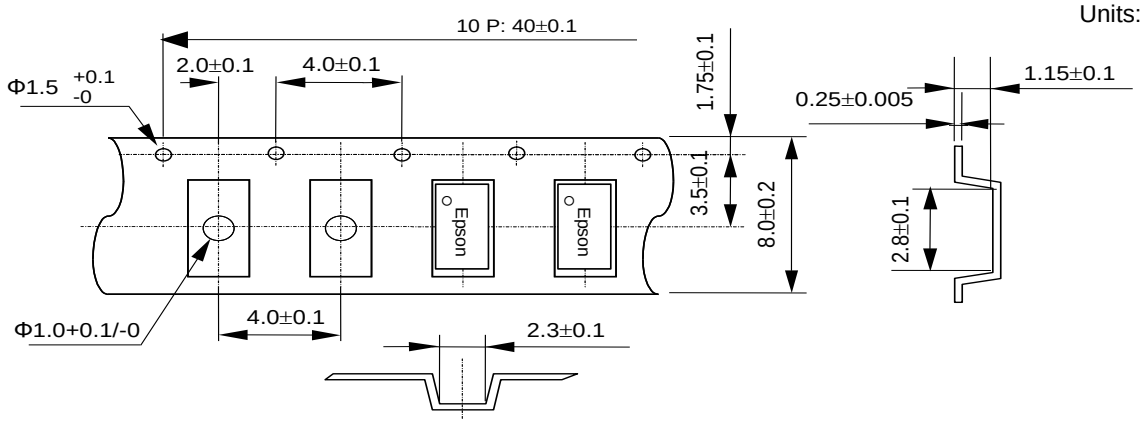
Subject to EIA-481, IEC-60286 and JIS C0806

1) Tape Dimensions

Carrier Tape Material: PS (Polystyrene)

Top Tape Material: PET (Polyethylene Terephthalate) + PE (Polyethylene)

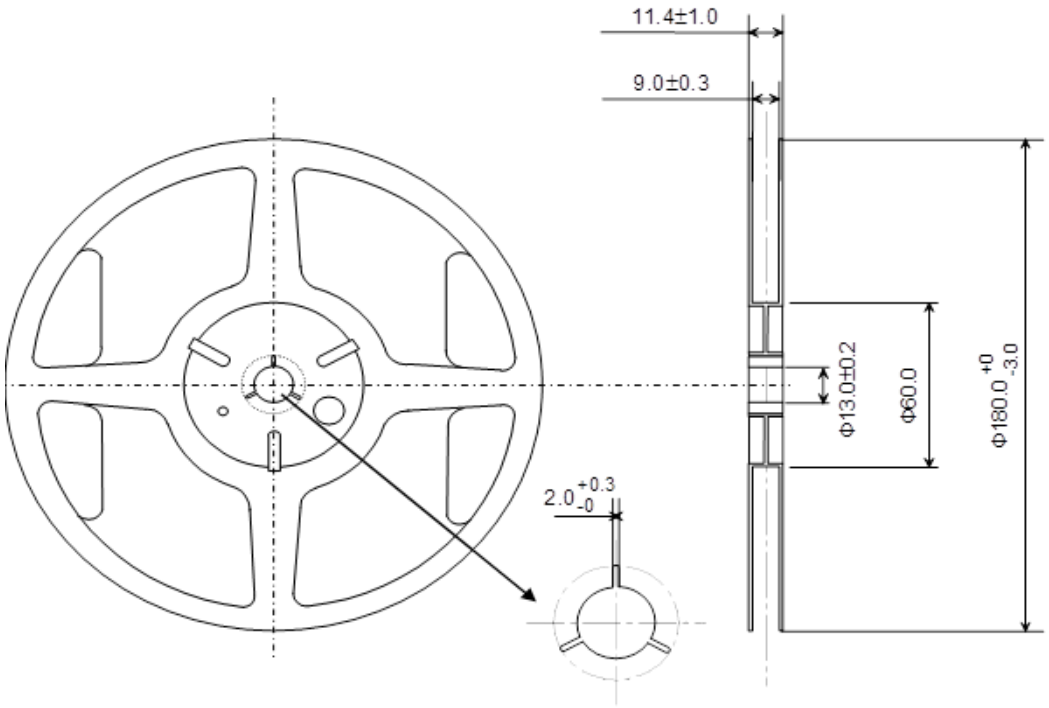
Units: mm




2) Reel Dimensions

Reel Material: PS (Polystyrene)

Units: mm




3) Storage Environment

We recommend to keep less than +30 °C and 85 %RH of humidity in a packed condition, and to use it less than 6 months after delivery.

[ 14 ] Handling Precautions

Prior to using this product, please carefully read the section entitled “Precautions” on our Web site (https://www5.epsondevice.com/en/information/#precaution) for instructions on how to handle and use the product properly to ensure optimal performance of the product in your equipment.
Before using the product under any conditions other than those specified therein, please consult with us to verify and confirm that the performance of the product will not be negatively affected by use under such conditions.
In addition to the foregoing precautions, in order to avoid the deteriorating performance of the product, we strongly recommend that you DO NOT use the product under ANY of the following conditions:

(1) Do not expose this product to excessive mechanical shock or vibration.
(2) This product can be damaged by mechanical shock during the soldering process depending on the equipment used, process conditions, and any impact forces experienced. Always follow appropriate procedures, particularly when changing the assembly process in any way and be sure to follow applicable process qualification standards before starting production.
(3) These devices are sensitive to ESD, use appropriate precautions during handling, assembly, test, shipment, and installation.
(4) The use of ultrasonic technology for cleaning, bonding, etc. can damage the Xtal unit inside this product. Please carefully check for this consideration before using ultrasonic equipment for volume production with this product.
(5) Noise and ripple on the power supply may have undesirable affects on operation and cause degradation of phase noise characteristics. Evaluate the operation of this device with appropriate power supplies carefully before use.
(6) When applying power, ensure that the supply voltage increases monotonically for proper operation. On power down, do not reapply power until the supplies, bypass capacitors, and any bulk capacitors are completely discharged since that may cause the unit to malfunction.
(7) Aging specifications are estimated from environmental reliability tests and expected frequency variation over time. They do not provide a guarantee of aging over the product lifecycle.
(8) The metal cap on top of the device is directly connected to the GND terminal. Take necessary precautions to prevent any conductor not at ground potential from contacting the cap as that could cause a short circuit to GND.
(9) To avoid any issues due to interference of other signal lines, please take care not to place signal lines near the product as this may have an adverse affect on the performance of the product.
(10) A bypass capacitor of the recommended value(s) must be connected between the $V_{CC}$ and GND terminals of the product. Whenever possible, mount the capacitor(s) on the same side of the PCB and as close to the product as possible to keep the routing traces short.
(11) Power supply connections to $V_{CC}$ and GND pins should be routed as thick as possible while keeping the high frequency impedance low in order to get the best performance.
(12) The use of a filter or similar element in series with the power supply connections to protect from electromagnetic radiation noise may increase the high frequency impedance of the power supply line and may cause the oscillator to not operate properly. Please verify the design to ensure sufficient operational margin prior to use.
(13) Keep PCB routing from the output terminal(s) to the load as short as possible for best performance.
(14) The Enable (OE/$\overline{OE}$/$\overline{ST}$/ST) input terminal is high impedance and so susceptible to noise. Connect it to a low impedance source when used and when not used it is recommended to connect it to Vcc for OE/$\overline{ST}$ inputs and GND for $\overline{OE}$/ST inputs.
(15) Do not short the output to GND as that will damage the product. Always use with an appropriate load resistor connected.
(16) This product should be reflowed no more than 3 times. If rework is needed after reflow, please correct it with a soldering iron with the tip set for a temperature of +350 °C or less and only contact each terminal once and for no more than 5 seconds. If this product is mounted on the bottom of the board during a reflow please check that it soldered down properly afterwards.

[Availability of mounting conditions]

| | |
|---|---|
| Reflow on the board | Available |
| Reflow under the board | The parts may fall. Please judge whether it is possible to implement. |
| Soldering pot/bath (Dip soldering system, Flow soldering system) | **Not Available** |
| Soldering iron | Available |

(17) Product failures during the warranty period only apply when the product is used according to the recommended operating conditions described in the specifications. Products that have been opened for analysis or damaged will not be covered. It is recommended to store and use in normal temperature and humidity environments described in the specifications to ensure frequency accuracy and prevent moisture condensation. If the product is stored for more than one year, please confirm the pin solderability prior to use.
(18) If the oscillation circuit is exposed to condensation, the frequency may change or oscillation may stop. Do not use in any conditions where condensation occurs.
(19) Do not store or use the product in an environment where it can be exposed to chemical substances that are corrosive to metal or plastics such as salt water, organic solvents, chemical gasses, etc. Do not use the product when it is exposed to sunlight, dust, corrosive gasses, or other materials for long periods of time.
(20) When using water-soluble solder flux make sure to completely remove the flux residue after soldering. Pay particular attention when the residues contain active halogens which will negatively affect the product and its performance.
(21) Terminals on the side of the product are internally connected to the IC, be careful not to cause short-circuits or reduce the insulation resistance of them in any way.
(22) Precautions for PLL cascade connection
This product uses a PLL (Phase Locked Loop) circuit to synthesize the required output frequency from the crystal oscillation. Therefore, if the output of this oscillator is further cascaded into a PLL, the jitter of the PLL may become large. Especially for applications such as image processing and communication synchronization, please be sure to check and approve it in advance.
(23) Should any customer use the product in any manner contrary to the precautions and/or advice herein, such use shall be done at the customer’s own risk.

## PROMOTION OF ENVIRONMENTAL MANAGEMENT SYSTEM CONFORMING TO INTERNATIONAL STANDARDS

At Seiko Epson, all environmental initiatives operate under the Plan-Do-Check-Action (PDCA) cycle designed to achieve continuous improvements. The environmental management system (EMS) operates under the ISO 14001 environmental management standard.

All of our major manufacturing and non-manufacturing sites, in Japan and overseas, completed the acquisition of ISO 14001 certification.

ISO 14000 is an international standard for environmental management that was established by the International Standards Organization in 1996 against the background of growing concern regarding global warming, destruction of the ozone layer, and global deforestation.

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In order provide high quality and reliable products and services than meet customer needs, Seiko Epson made early efforts towards obtaining ISO9000 series certification and has acquired ISO9001 for all business establishments in Japan and abroad. We have also acquired IATF 16949 certification that is requested strongly by major manufacturers as standard.

IATF 16949 is the international standard that added the sector-specific supplemental requirements for automotive industry based on ISO9001.

■ Explanation of marks used in this datasheet

| | |
|---|---|
| Pb Free | **●Pb free.** |
| RoHS Compliant | **●Complies with EU RoHS directive.**<br>*About the products without the Pb-free mark.<br>Contains Pb in products exempted by EU RoHS directive<br>(Contains Pb in sealing glass, high melting temperature type solder or other) |

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