Clock OSC XG-2121CA

Product name XG-2121CA 133.000000MHz +/-50ppm PGRN

Product Number / Ordering code X1M0003110007xx

Please refer to the 9.Packing information about xx (last 2 digits)

Output waveform LV-PECL

Pb free / Complies with EU RoHS directive

Reference weight Typ. 133 mg

1.Absolute maximum ratings

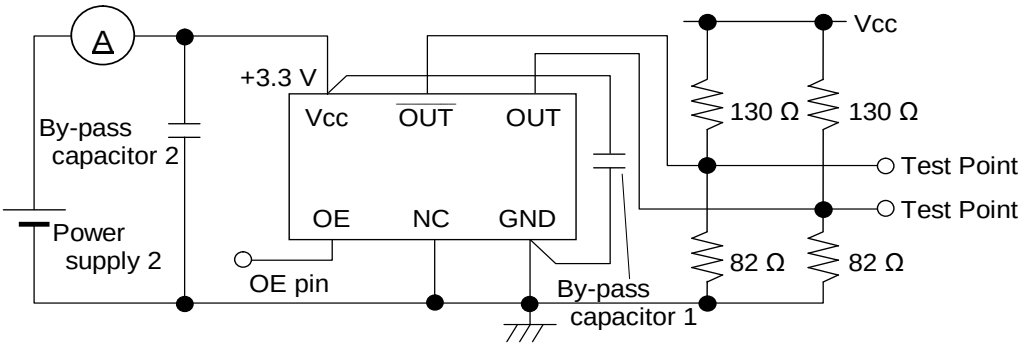
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions / Remarks
Maximum supply voltage	Vcc-GND	-0.5	-	4	V	-
Storage temperature	T_stg	-55	-	125	ºC	Storage as single product
Input voltage	Vin	-0.5	-	Vcc+0.5	V	ST or OE Terminal

2.Specifications(characteristics)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions / Remarks
Output frequency	f0	-	133.0000	-	MHz	
Supply voltage	Vcc	2.375	2.5	2.625	V	-
Operating temperature	T_use	-5	-	85	ºC	-
Frequency tolerance	f_tol	-50	-	50	$x10^{-6}$	-
Current consumption	Icc	-	-	60	mA	OE=Vcc,L_ECL=50ohm
Stand-by current	I_std	-	-	-	mA	-
Disable current	I_dis	-	-	2.0	mA	OE=GND
Symmetry	SYM	45	-	55	%	As output crodding point
Output voltage(LV-PECL)	V_{OH}	Vcc-1.025	1.55	Vcc-0.88	V	-
	V_{OL}	Vcc-1.81	0.8	Vcc-1.62	V	-
Output load condition(ECL)	L_ECL	-	50	-	Ω	Terminated to Vcc-2.0V
Input voltage	V_{IH}	30% Vcc	-	-		OE Terminal
	V_{IL}	-	-	30% Vcc		OE Terminal
Rise time	t_r	-	-	400	ps	At 20% to 80% output swing
Fall time	tf	-	-	400	ps	At 20% to 80% output swing
Start-up time	t_str	-	-	10	ms	-
Jitter	t_{DJ}	-	-	N/A	ps	Deterministic Jitter
	T_{RJ}	-	-	N/A	ps	Random Jitter
	t_{RMS}	-	-	N/A	ps	δ(RMS of total distribution)
	t_{p-p}	-	-	N/A	ps	Peak to Peak
	t_{acc}	-	-	N/A	ps	Accumulated Jitter(δ) n=2 to 50000 cycles
Phase jitter	t_{PJ}	-	-	0.23	ps	Off set Frequency: 12kHz to 20MHz
Phase noise	L(f)	-	-	-	dBc/Hz	Off set 1Hz
		-	-49.6	-	dBc/Hz	Off set 10Hz
		-	-78.1	-	dBc/Hz	Off set 100Hz
		-	-106.2	-	dBc/Hz	Off set 1kHz
		-	-141.0	-	dBc/Hz	Off set 10kHz
		-	-148.7	-	dBc/Hz	Off set 100kHz
		-	-152.5	-	dBc/Hz	Off set 1MHz
Frequency aging	f_age	-10	-	10	$x10^{-6}$/Year	@+25ºC first year

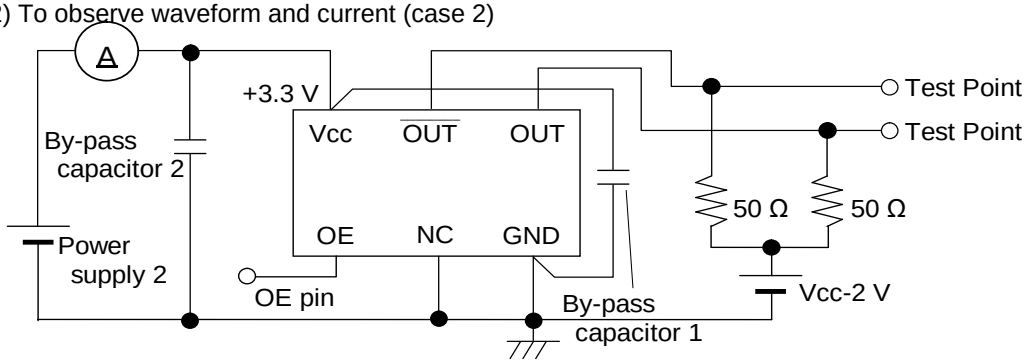
3.Test circuit

1) To observe waveform and current (case 1)



* The lines from OUT and $\overline{OUT}$ pin are same length.
* To measure the disable current, OE pin is connected to GND

2) To observe waveform and current (case 2)



* The lines from OUT and $\overline{OUT}$ pin are same length.
* To measure the disable current, OE pin is connected to GND

3) Measurement condition

A) Oscilloscope
- •Bandwidth should be 5 times higher than DUT's output frequency (4 GHz).
- •Probe ground should be placed closely from test point and lead length should be as short as possible.

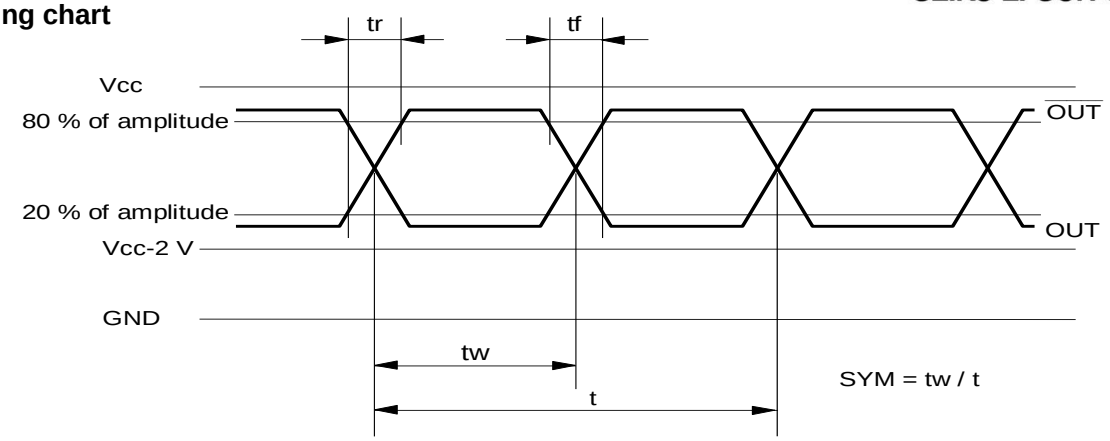
B) By-pass capacitor 1 (approx. 0.01 µF to 0.1 µF) places closely between Vcc and GND.

C) By-pass capacitor 2 (approx. 10 µF) places closely between power supply terminals on the board.

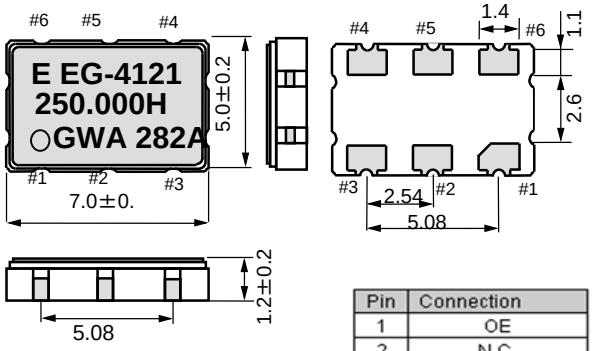
D) Use the current meter whose internal impedance value is small.

E) Power supply
- • Start up time (0 Vg90 %Vcc) of power source should be more than 150 µs and slew rate should be less than 19.8 mV/µs.
- • Impedance of power supply should be as low as possible.

4.Timing chart

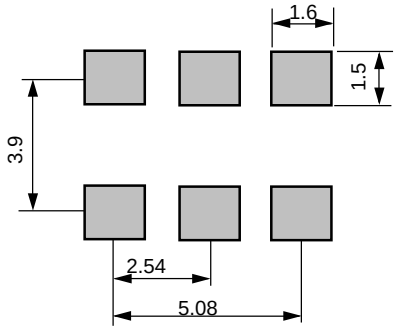


5.External dimensions (Unit: mm)



Pin	Connection
1	OE
2	N.C.
3	GND
4	OUT
5	$\overline{OUT}$
6	VCC

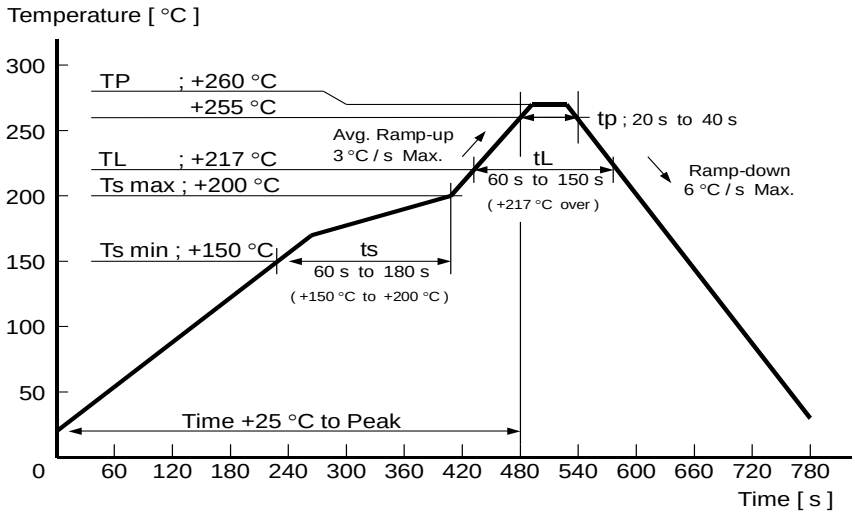
6.Footprint(Recommended) (Unit: mm)



To maintain stable operation, provide a 0.01uF to 0.1uF by-pass capacitor at a location as near as possible to the power source terminal of the crystal product (between Vcc - GND).

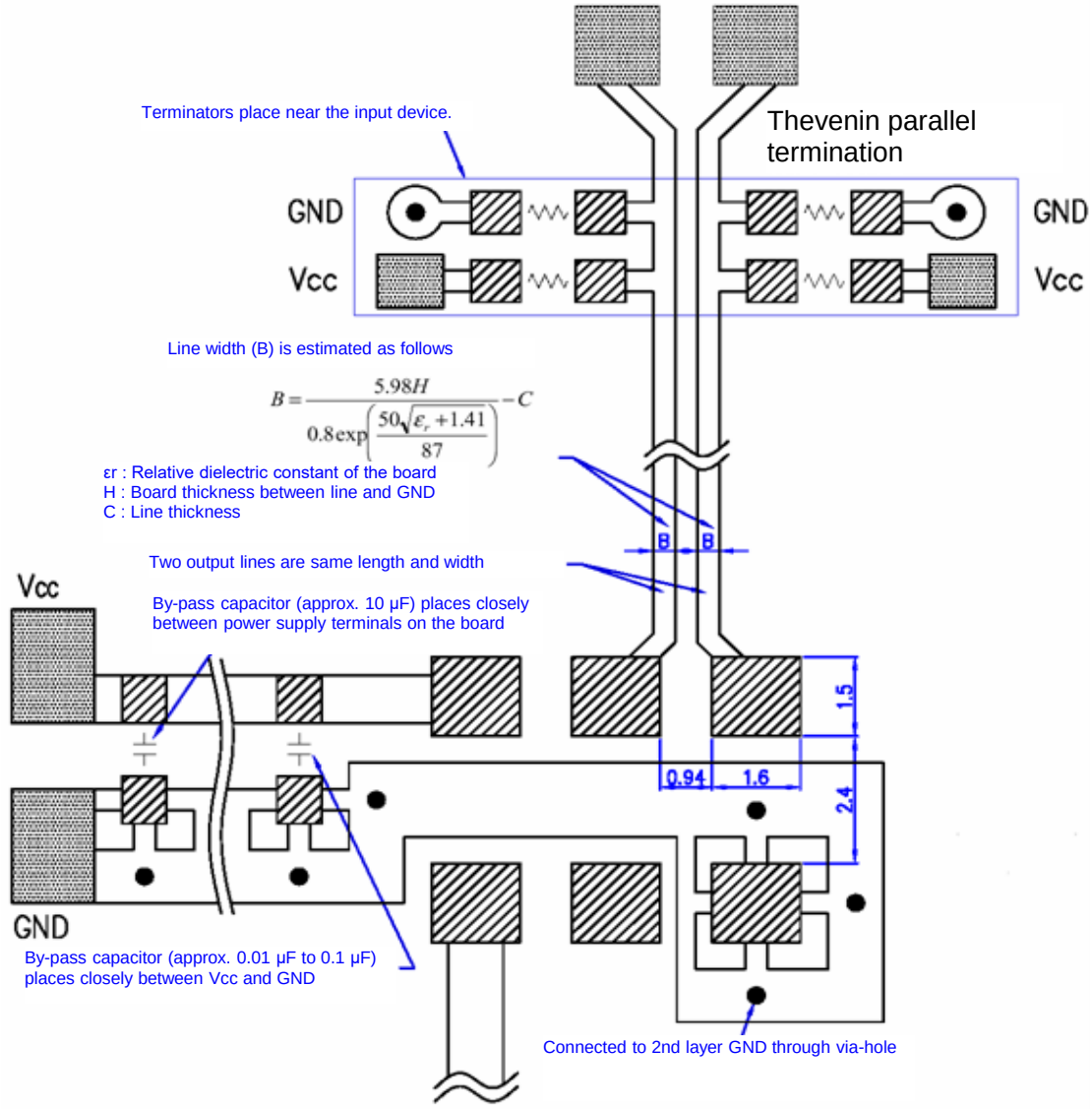
7.Reflow profile

Reflow condition (Follow of JEDEC STD-020D.01)



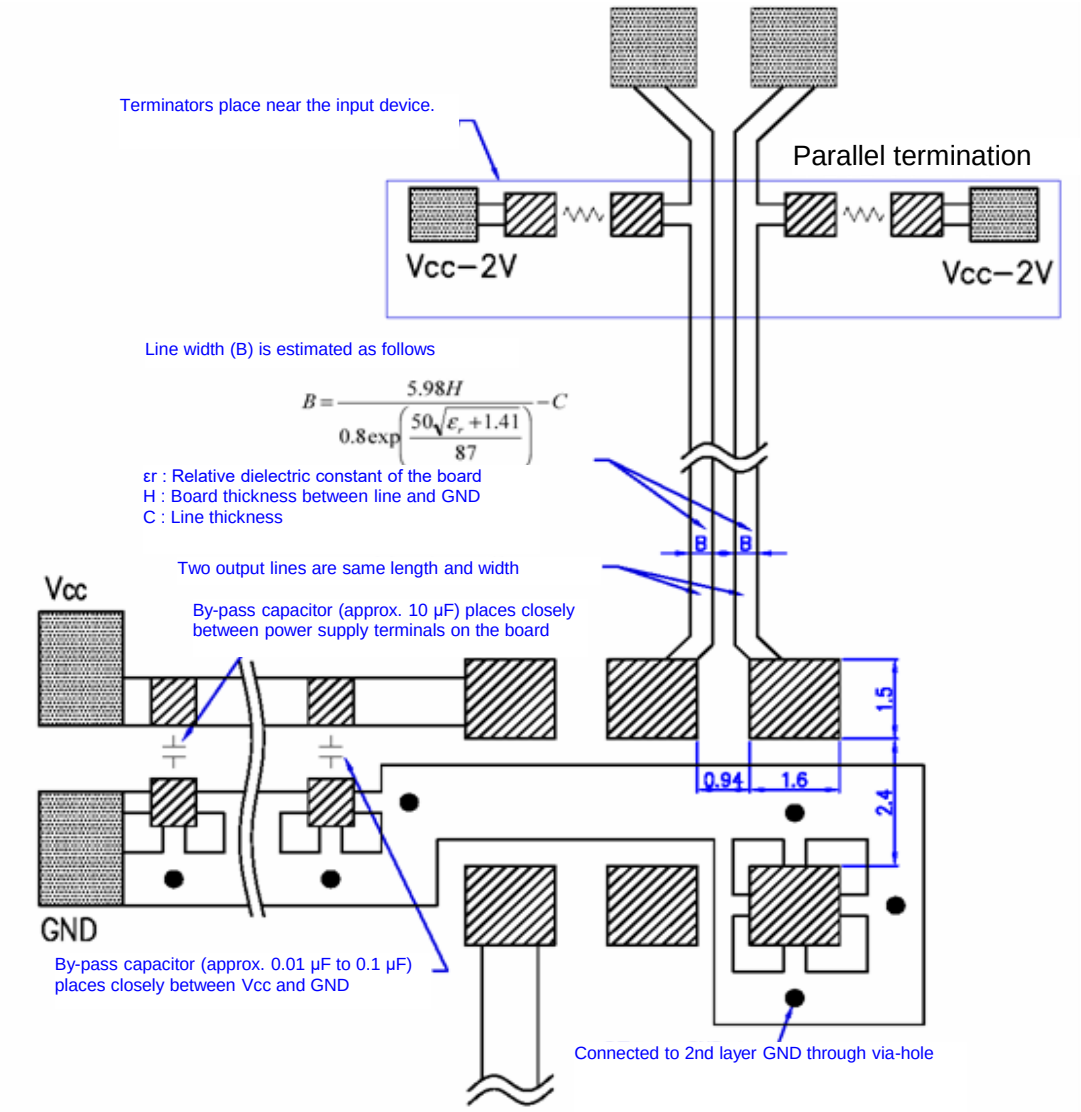
8.PCB layout (2 layers, 2nd layer is all GND pattern)

Case 1



* By-pass capacitor (approx. 0.01 µF to 0.1 µF) places closely between Vcc and GND.
* By-pass capacitor (approx. 10 µF) places closely between power supply terminals on the board.
* Please design the two output lines by characteristic impedance 50 Ω and same length, and try to make the output lines as short as possible.
* Terminators place near the input device.

Case 2



* By-pass capacitor (approx. 0.01 µF to 0.1 µF) places closely between Vcc and GND.
* By-pass capacitor (approx. 10 µF) places closely between power supply terminals on the board.
* Please design the two output lines by characteristic impedance 50 Ω and same length, and try to make the output lines as short as possible.
* Terminators place near the input device.

9.Packing information

[1]Product number last 2 digits code(xx) description The recommended code is "00"

X1M0003110007xx

Code	Condition	Code	Condition
01	Any Q'ty vinyl bag(Tape cut)	13	500pcs / Reel
11	Any Q'ty / Reel	00	1000pcs / Reel
12	250pcs / Reel		

[2] Taping specification

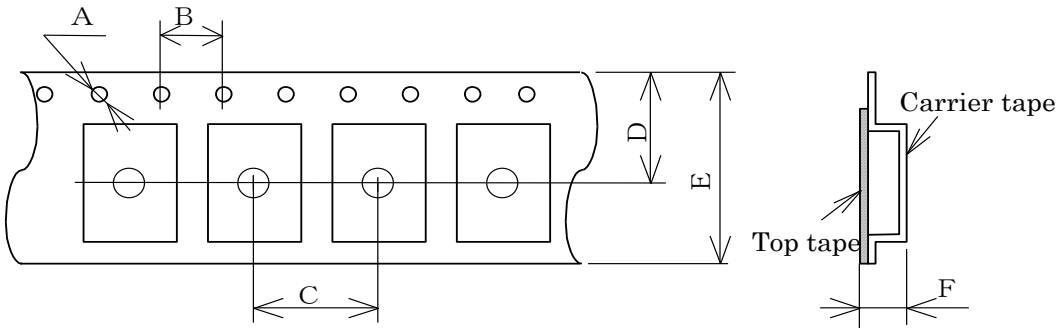
Subject to EIA-481 & IEC-60286

(1) Tape dimensions

Material of the Carrier Tape : PS

Material of the Top Tape : PET+PE

Unit: mm

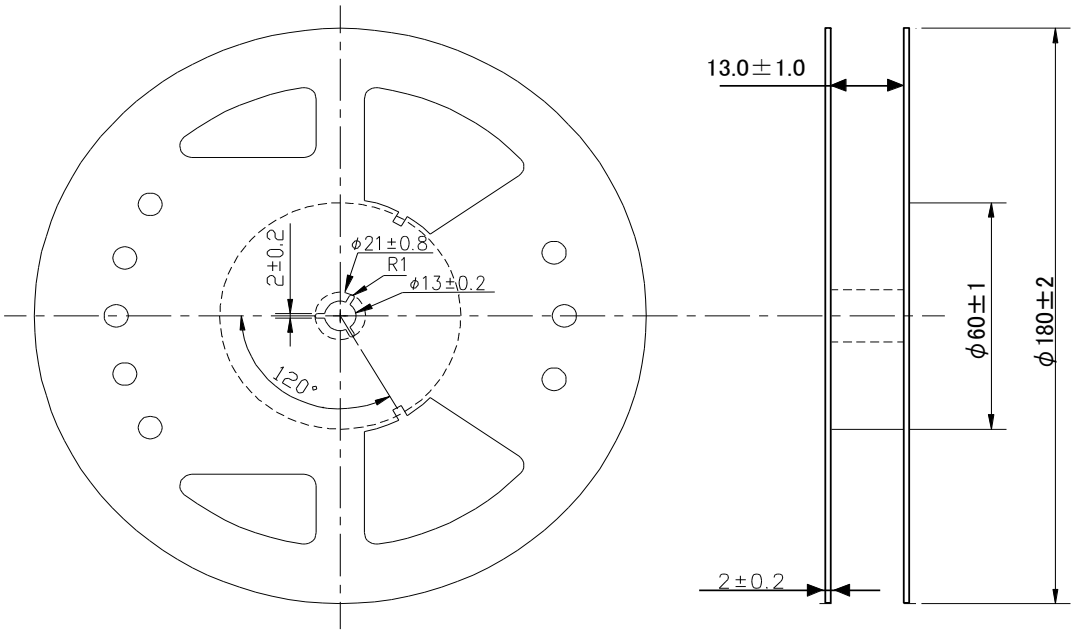


Symbol	A	B	C	D	E	F
Value	φ1.5	4	8	9.25	16	2.3

(2) Reel dimensions

Center material : PS

Material of the Reel : PS



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