VCXO VG7050CDN

SEIKO EPSON CORPORATION

Product name VG7050CDN 150.000000MHz CJGHBA
Product code / Ordering code X1G0048610010xx
Please refer to the 8.Packing information about xx (last 2 digits)

Output waveform CMOS
Complies with EU RoHS directive
Reference weight Typ.169mg

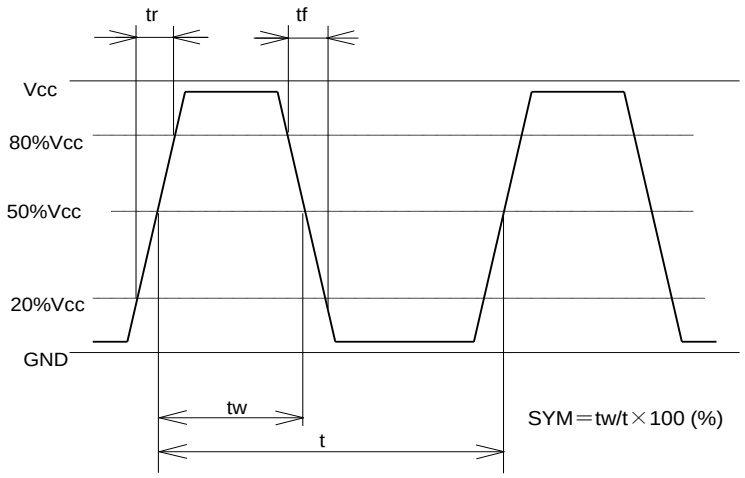
1.Absolute maximum ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions / Remarks
Maximum supply voltage	Vcc-GND	-0.3	-	+5	V	-
Storage temperature	T_stg	-55	-	+125	ºC	Storage as single product after unpacking.
Input voltage	Vin	-0.3	-	Vcc+0.3	V	Vc traminal

2.Specifications(characteristics)

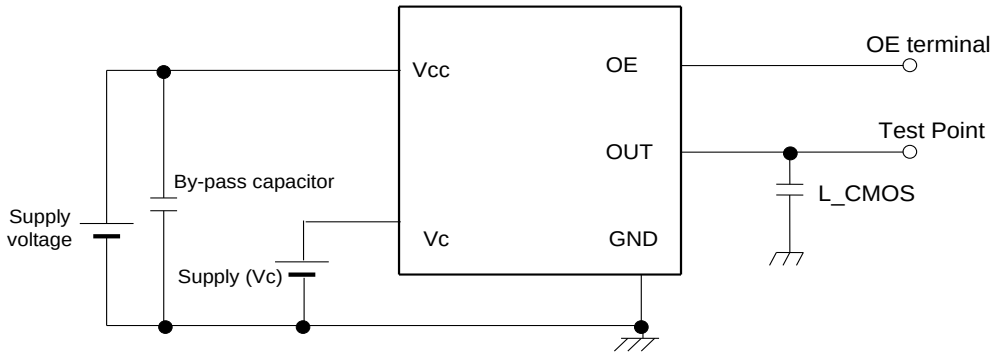
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions / Remarks
Output frequency	f0		150.0000		MHz	
Supply voltage	Vcc	3.135	3.3	3.465	V	-
Control voltage	Vc	0	1.65	3.3	V	Vc=1.65V+/-1.65V
Operating temperature	T_use	-40	-	+85	ºC	-
Frequency tolerance	f_tol	-50	-	+50	$x10^{-6}$	T_Use
Current consumption	Icc	-	-	30	mA	-
Disable current	I_dis	-	-	-	mA	OE=GND
Frequency control range	f_cont	+/-100	-	-	$x10^{-6}$	-
Absolute pull range	APR	+/-50	-	-	$x10^{-6}$	-
Modulation characteristics	BW	10	-	-	kHz	+/-3dB
Input resistance	Rin	10	-	-	MΩ	Vc terminal
Linearity	F_{LIN}	-	-	+/-10	%	-
Frequency change polarity	-		Positive		–	-
Symmetry	SYM	45	-	55	%	50%Vcc level
Output voltage	V_{OH}	90%Vcc	-	-	V	-
	V_{OL}	-	-	10%Vcc	V	-
Output load condition	L_CMOS	-	-	15	pF	-
Input voltage	V_{IH}	70%Vcc	-	-	V	-
	V_{IL}	-	-	30%Vcc	V	-
Rise time	tr	-	-	2	ns	20%Vcc to 80%Vcc level
Fall time	tf	-	-	2	ns	80%Vcc to 20%Vcc level
Start-up time	t_str	-	-	10	ms	t=0 at 90%Vcc
Phase jitter	tPJ	-	-	1	ps	Offset frequency:12 kHz to 20 MHz
Frequency aging	f_aging	-	-	-	$x10^{-6}$	Included in frequency tolerance

3.Timing chart

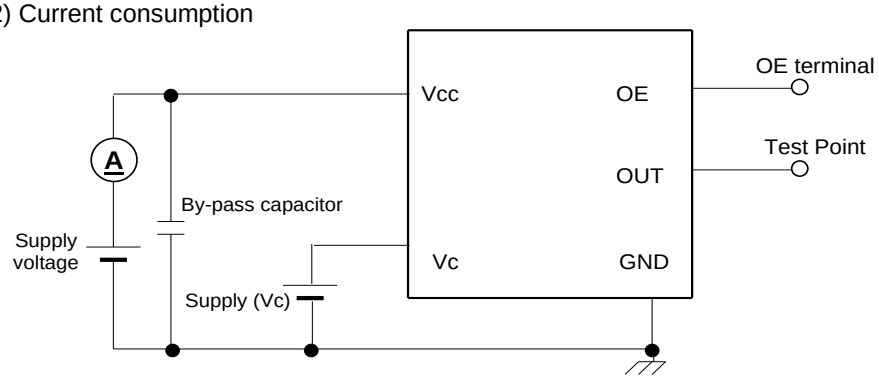


4.Test circuit

1) C-MOS load CL=15 pF



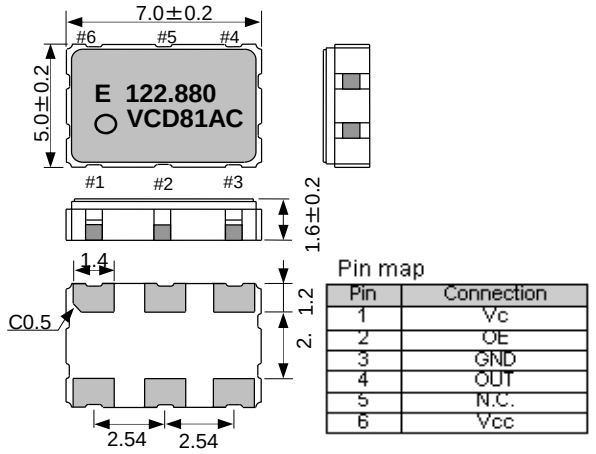
2) Current consumption



3) Condition

1. Oscilloscope
   Bandwidth should be 5 times higher than DUT's output frequency.
   Probe ground should be placed closely from test point and lead length should be as short as possible.
2. L_CMOS includes probe capacitance.
3. By-pass capacitor (0.1 µF + 10 µF) is placed closely between Vcc and GND.
4. Use the current meter whose internal impedance value is small.
5. Power Supply
   ・Start up time (0 %Vcc→90 %Vcc) of power source should be more than 150 µs.
   ・Impedance of power supply should be as low as possible.

5.External dimensions (Unit: mm)

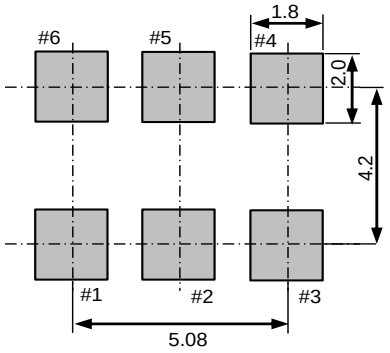


Pin map

Pin	Connection
1	Vc
2	OE
3	GND
4	OUT
5	N.C.
6	Vcc

OE pin = "H" or "open": Specified frequency output.
OE pin = "L" : Output is high impedance.

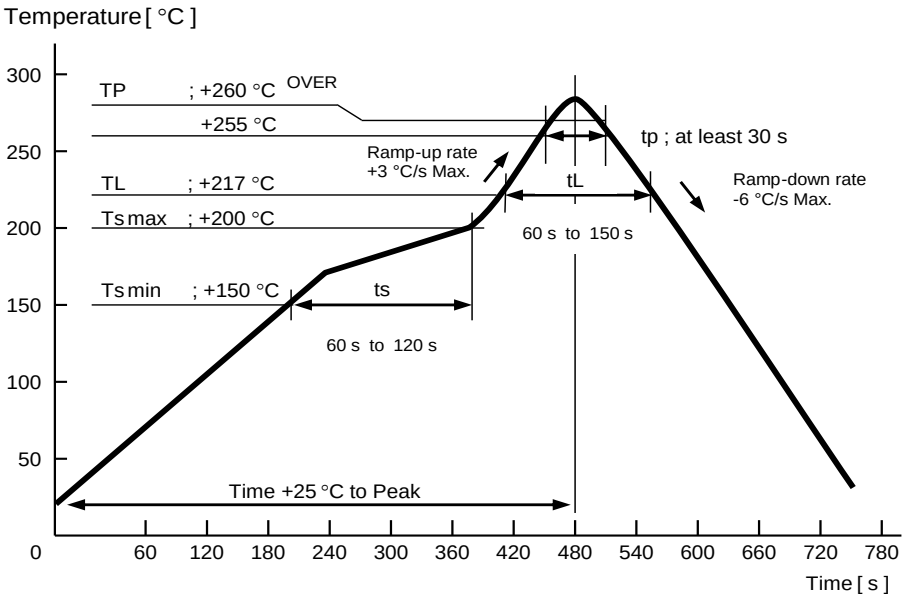
6.Footprint(Recommended) (Unit: mm)



To maintain stable operation, provide a 0.1µF + 10µF by-pass capacitor at a location as near as possible to the power source terminal of the crystal product (between Vcc - GND).

7.Reflow profile

JEDEC STD-020D.01



8.Packing information

[1]Product number last 2 digits code(xx) description The recommended code is "00"

X1G0048610010xx

Code	Condition
00	1000pcs / Reel
01	Any Q'ty vinyl bag(Tape cut)
11	Any Q'ty / Reel

[2] Taping specification

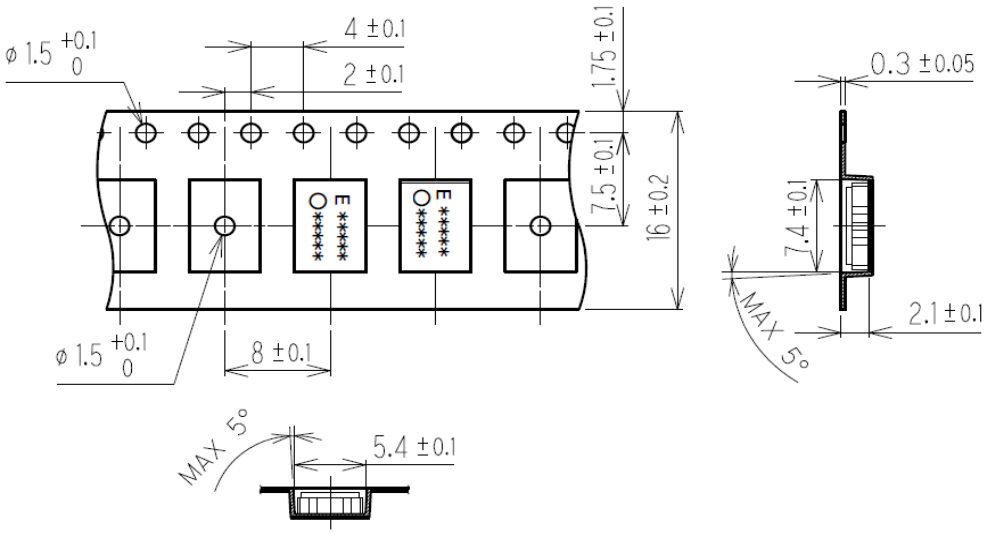
Subject to EIA-481 & IEC-60286

(1) Tape dimensions

Material of the Carrier Tape : PS

Material of the Top Tape : PET+PE

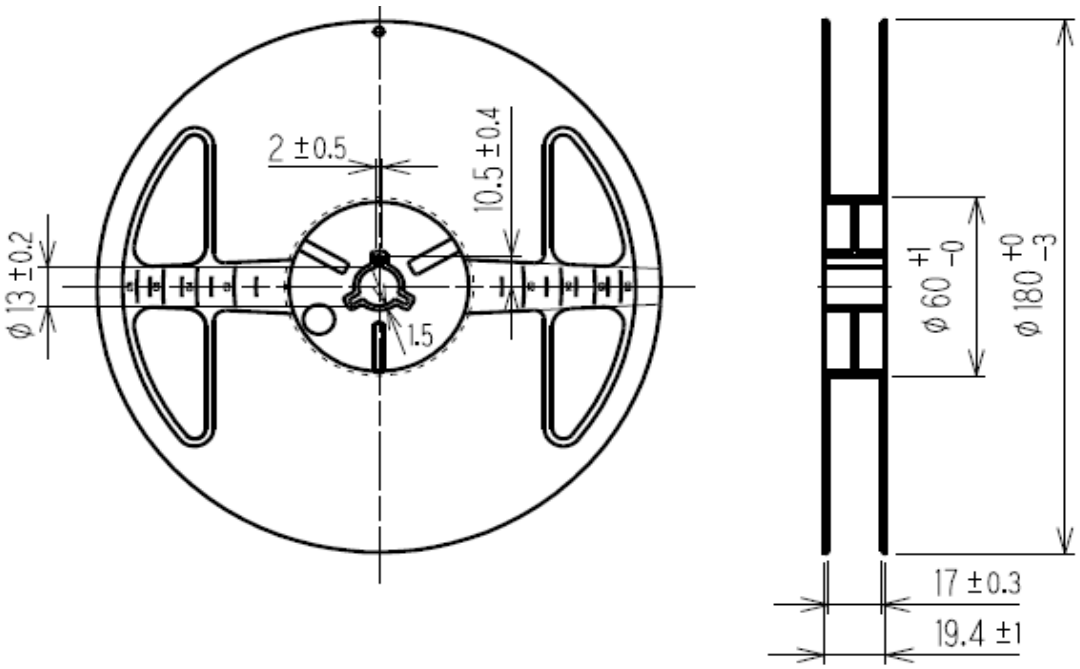
Unit: mm



(2) Reel dimensions

Material of the Reel : PS

Unit: mm



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