Preliminary Specifications

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Temperature Compensated Crystal Oscillator (VC-TCXO)

TG-5021CG 52 MHz

- Reflowable and high density mounting type ultra small size SMD (2.5×2.0×0.9 mm).
- Using the heat-resisting type AT cut quartz crystal
  allows almost the same temperature soldering as universal SMD IC.
- Operating supply voltage : Vcc 1 = 2.4 V / Vcc 2 = 2.775 V.

■ Specifications

1. Absolute maximum ratings

Parameter	Symbol	Value	Unit	Note
Supply voltage	V_{CC}-GND	-0.3 to 4.5	V	
Frequency control voltage	Vc	-0.3 to V_{CC}+0.3	V	V_C Terminal
Storage temperature range	$T_{_STG}$	-40 to +90	°C	

2. Operating range

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power voltage		$V_{CC}1$	2.28	2.4	2.52	V	Vcc=2.4V+/-0.12V
		$V_{CC}2$	2.64	2.775	2.91		Vcc=2.775V +/-0.135V
		GND	0.0	0.0	0.0	V	
Frequency control voltage		Vc	0.25	1.0	1.75	V	V_C Terminal
Operating temperature range		T_use	-30	+25	+85	°C	
Output load		Load_R	9	10	11	kΩ	
		Load_C	9	10	11	pF	
	DC-cut capacitor	C_C	0.01			μF	

DC-cut capacitor is not included in our TCXO. Please insert DC-cut capacitor in output line.

DO NOT COPY

Confidential
Until: Permanent

3.Frequency characteristics

1) Output frequency 52.000000 MHz

2) Frequency characteristics

(Condition : V_{CC}=2.4 V or 2.775 V, Vc=1.0 V, GND=0.0 V, Load 10kΩ//10pF(DC cut), T_use =+25°C)

Parameter	Symbol	Value	Unit	Note
Frequency tolerance .	f_tol	+/- 0.8×10^{-6} Max.	-	T_use =+25 °C +/-2 °C Before reflow cycles
	f_tol(OSC)	+/- 1.5×10^{-6} Max.	-	T_use =+25 °C +/-2 °C Reflow cycles : 2 times.*1*2
Frequency / temperature Characteristics	fo-Tc	+/- 2.0×10^{-6} Max.	-	T_use =-30 °C to +85 °C Based on frequency at +25 °C
Frequency / Load coefficient	fo-Load	+/- 0.2×10^{-6} Max.	-	Load :10 kΩ//10 pF +/-10 % each
Frequency / voltage coefficient	fo-Vcc	+/- 0.1×10^{-6} Max.	-	Vcc=2.4V +/- 0.12V Vcc=2.775V +/- 0.135V
Frequency ageing	f_age	+/- 2.0×10^{-6} Max.	-	T_use =+25 °C 1 year
		+/- 5.0×10^{-6} Max.	-	T_use =+25 °C 10 years

*1 Include initial frequency tolerance and frequency deviation after reflow cycles.
*2 Measurement of frequency deviation is made 2h after reflow soldering.

3) Frequency adjustment characteristics

(Condition : V_{CC}=2.4 V or 2.775 V, Vc=1.0 V, GND=0.0 V, Load 10kΩ//10pF(DC cut), T_use =+25°C)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Frequency control range	fcont	-15×10^{-6}		-10×10^{-6}	-	Vc=0.25 V
		+10×10^{-6}		+15×10^{-6}		Vc=1.75 V
Transfer function	-	Positive			-	
Input impedance (V_C terminal)	Rin	500			KΩ	V_C-GND(DC Level)
Input capacitance (V_C terminal)	Cin			10	pF	

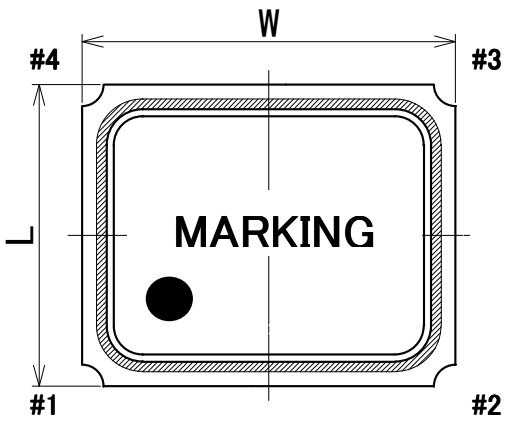
4.Electrical characteristics

(Condition : V_{CC}=2.4 V or 2.775 V, Vc=1.0 V, GND=0.0 V, Load 10kΩ//10pF(DC cut), T_use =+25°C)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Current consumption	Icc			2.0	mA	
Output level	Vpp	0.8		2.0	V	Peak to peak voltage Clipped sine wave
Symmetry	SYM	45		55	%	GND Level
Harmonics	-		-45	-20	dBc	2nd harmonic
			-17	-13		3rd harmonic
			-65	-50		17th harmonic
				-50		49th harmonic
Start up time	tosc			3.0	ms	Output level = 90 %
				3.0		Within ±2ppm of final frequency
				1.5		Within ±20ppm of final frequency
SSB Phase noise (T_use =+25°C)	L(f)		-110 -131 -147 -151 -151	-100 -125 -142 -147 -148	dBc/Hz	Offset:100Hz Offset:1kHz Offset:10kHz Offset:100kHz Offset:1MHz
SSB Phase noise (T_use = -30 to +85°C)	L(f)		-105 -126 -145 -150 -151	-100 -123 -142 -147 -148	dBc/Hz	Offset:100Hz Offset:1kHz Offset:10kHz Offset:100kHz Offset:1MHz

5. OUTLINE DRAWING

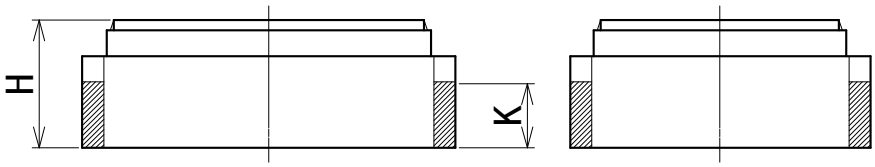
[TOP VIEW]



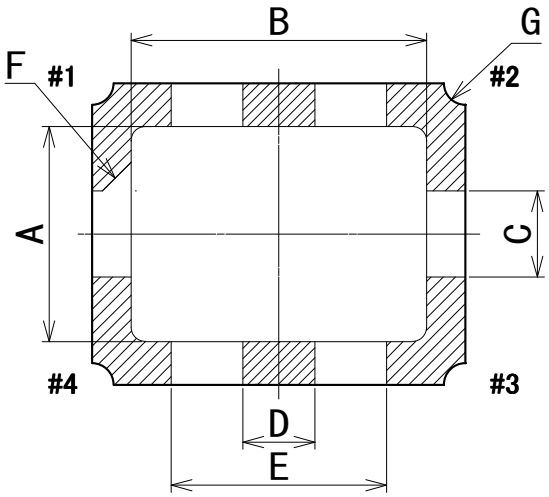
Marking
TBD

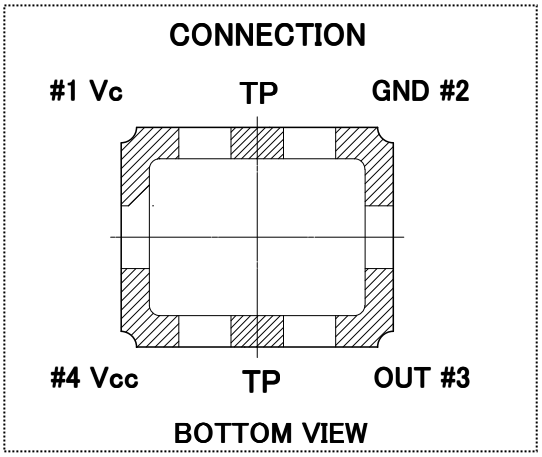
Material
Ceramics (base)
Au coated nickel (terminal)
Fe-Ni-Co (lid)

[SIDE VIEW]



[BOTTOM VIEW]

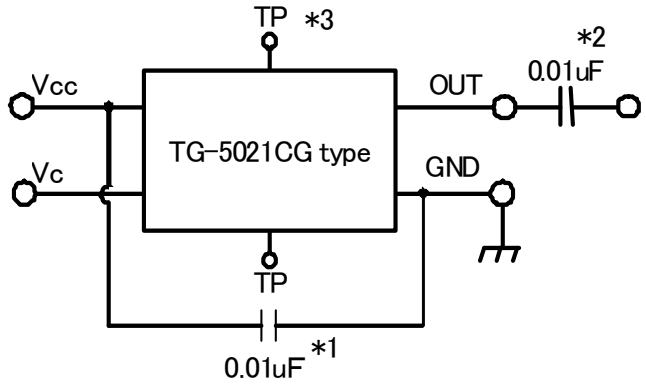




(unit : mm)

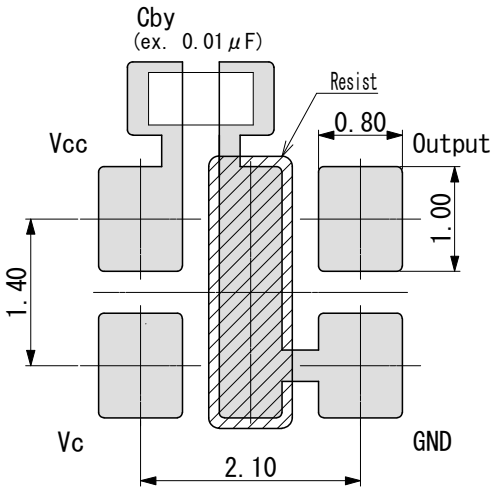
DIM.	MIN.	TYP.	MAX.	DIM.	MIN.	TYP.	MAX.
W	2.30	2.50	2.70	D	0.40	0.50	0.60
L	1.80	2.00	2.20	E	1.35	1.50	1.65
H	0.70	0.80	0.90	F	---	C0.2	---
A	1.35	1.50	1.65	G	---	R0.15	---
B	1.95	2.10	2.25	K	---	0.45	---
C	0.50	0.60	0.70				

6. CONNECTION



***1 Please connect capacitor(recommendation:0.01 μF) between "Vcc" and "GND" terminal.**
***2 Please connect capacitor(recommendation:0.01 μF) between "OUT" terminal and load.**
***3 Do not connect "TP" terminal.**
***4 This product has one chip LSI. Do not supply over +4.5V or negative voltage under −0.3V to "Vcc" terminal. Do not supply over Vcc+0.3V or negative voltage under −0.3V to "Vc" terminal. Do not supply any voltages to "OUT" terminal.**
***5 Do not supply any voltages in any way which differs from the above connection figure.**
***6 Do not open "Vc" terminal.**

7. Recommended soldering pattern



Except for this recommended soldering pattern, please contact us for inquiries.