Technical specifications

High-precision Yaw sensor: XV7181BB

Seiko Epson Corporation

Microdevices Operations Division

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The specification values described in this manual are provisional specifications.

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Revision history

Rev. No.	Date of revision	Page	Revised content
1.0	Sept. 21, 2023	All	New Release.

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Symbols

	• **A lead-free product.**
	• **Compliant with the EU RoHS directive.** * About products without the Pb-Free label Product terminals are lead-free but the internal components of the product contain lead (high melting point solder lead as well as the lead contained in the glass of an electronic component are both not applicable under the EU RoHS directive).
	• **Indicates a product intended for use in an automobile (body, information systems, etc.). The product has been designed and manufactured in accordance with a quality assurance program suited for the on-board environment of an automobile.**
	• **Indicates a product intended for use to further the safe operation of an automobile (driving, stopping, turning). The product has been designed and manufactured in accordance with a quality assurance program suited for the on-board safety of an automobile.**

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1. Block Diagram

The block diagram of the sensor is shown in Figure 1.1.

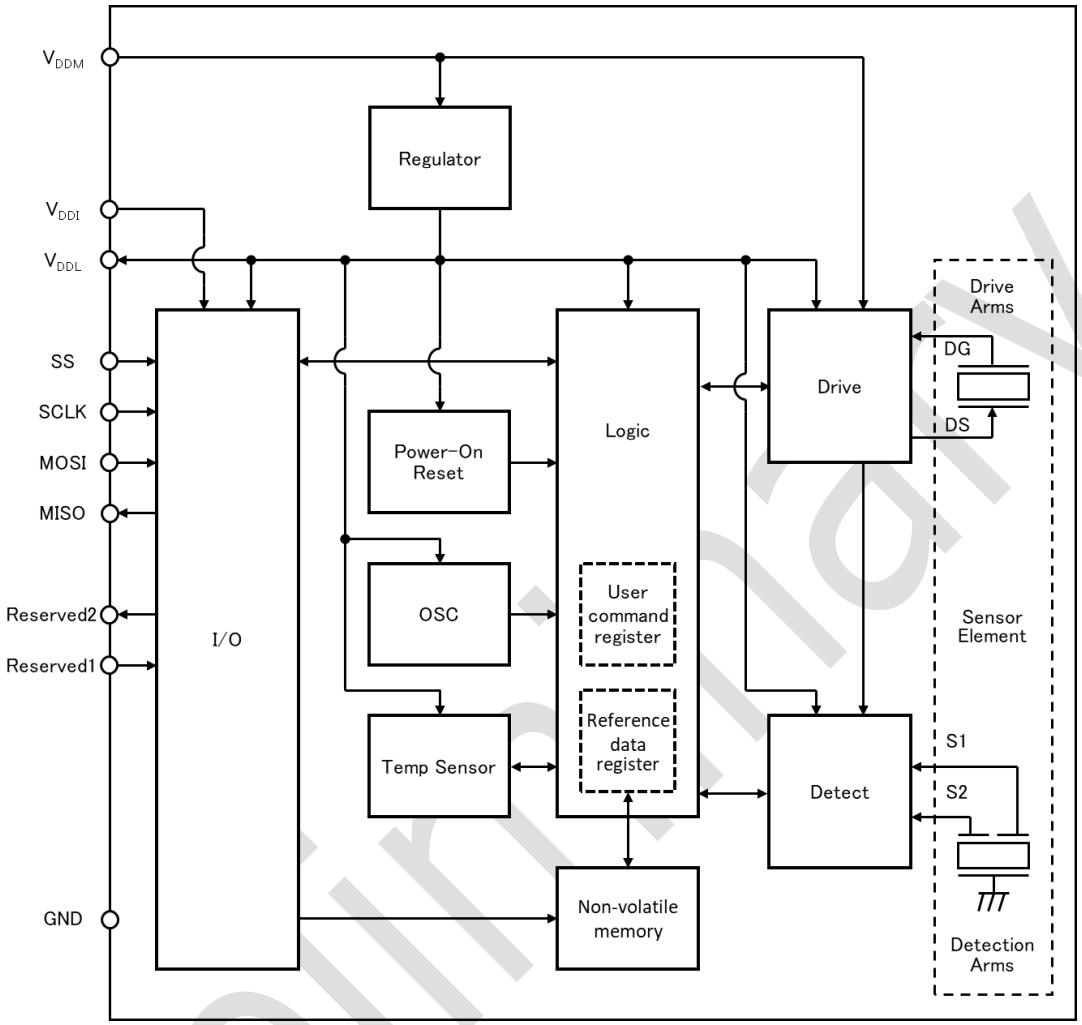


Figure 1.1 Functional Block Diagram

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2. Function Explanation

2.1. Detection Axis and Output Polarity

This product detects an angular rate of a rotational movement. The correlation between a detecting axis of the angular rate and an output polarity is shown in Figure 2.1.

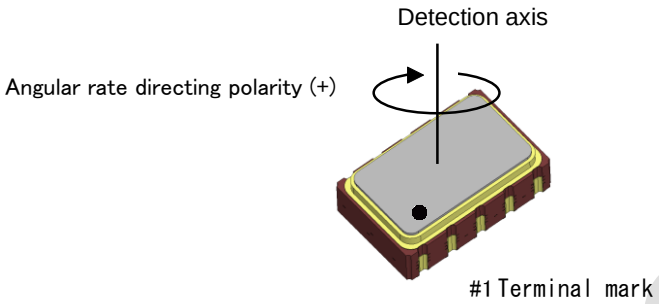


Figure 2.1 Detection Axis and Detection Polarity

2.2. Interface

This product is compatible with SPI (4-wire, 3-wire) and I²C. This sensor allows for interface power supply voltage settings (V_{DDI}) that are independent of the power supply voltage (V_{DDM}) to enable communications with interfaces of various logic levels.

2.3. Angular Rate Output

The angular rate output data is provided in the 2's compliment expression. 16 bits or 24 bits can be selected from the register settings. The AD converter sampling frequency f_s is 12.000 kHz for frequency symbol J.

The angular rate output data can also be provided after processing through the low-pass filter (LPF). In addition, the Notch Filter (NF) is available and can be enabled to suppress residual output of detuning frequency after mechanical shock. Regarding the Digital Filter, See the Chapter 8.

LPF: This is a 2nd, 3rd or 4th order filter, the cutoff frequency can be selected.
(1/10/25/50/100/200/400/500 [Hz])

NF: Either enable or disable can be selected. The center frequency of the Notch Filter is already set at our factory individually.

2.4. Temperature sensor output

Temperature output data is provided in the 2's compliment expression. The temperature output in the zero code can be selected by the register setting. See the Sector 6.5.

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3. Electrical Characteristics

3.1. Absolute Maximum Rating

Table 3.1 Absolute Maximum Ratings

Parameter	symbol	Min.	Type.	Max.	unit	Comdition
Supply voltage	V_{DDM}	-0.3	-	+4.0	IN	GND = 0 V
Supply voltage for interface	V_{DDI}	-0.3	-	+4.0	IN	GND = 0 V
Storage temperature	T_{STG}	-40	-	+85	°C	
Conditions for soldering	-	+350 °C, 3 s			-	

3.2. Operating Conditions

Table 3.2 Operating conditions

Parameter	Symbol	Min.	Type.	Max.	Unit	Condition
Supply voltage	V_{DDM}	+2.7	-	+3.6	IN	GND = 0 V
Supply voltage for interface	V_{DDI}	+1.65	-	+3.6	IN	GND = 0 V
Operating temperature	T_{OPR}	-40	-	+85	°C	
Supply voltage start-up time	t_{pu}	0.01	-	100	ms	V_{DDM} 0 % to 90 %
4-WireSPI clock frequency	f_{SCLK}	-	-	10	MHz	V_{DDI} > +2.4 V
4-WireSPI clock frequency	f_{SCLK}	-	-	5	MHz	IN_{DDI} ≤ +2.4 V
3-WireSPI clock frequency	f_{SCLK}	-	-	5	MHz	
I^2C clock frequency	f_{SCL}	-	-	400	kHz	
Sampling frequency	f_s	-	12.000	-	kHz	Frequency codel: J

(Note) Using the drive frequency integral multiplier as communications clock may result in fluctuations in the angular rate output.

(Note) Acquiring angular rate data as a frequency that is a fraction of the integer for the drive frequency can result in fluctuations in the angular rate output.

3.3. DC Characteristics

Table 3.3 DC Characteristic

(V_{DDM} = 2.7 V to 3.6V, V_{DDI} = 1.65 V to 3.6 V, GND = 0 V, T_{OPR} = -40 °C to +85 °C)

parameter	symbol	Min.	Type.	Max.	Unit	Condition
Logic input voltage	V_{IH}	V_{DDI}× 0.7	-	-	V	
	IN_{THE}	-	-	V_{DDI}× 0.3	V	
Logic output voltage	V_{OH}	V_{DDI}- 0.4	-	-	V	V_{DDI}= Min., Load +1 mA
	IN_{OL}	-	-	+0.4	V	V_{DDI}= Min., Load -1 mA

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3.4. Operating Sequence at Start-Up

Table 3.4 Operating Sequence at Start-Up

V_{DDM} = 2.7 V to 3.6 V, V_{DDI} = 1.65 V to 3.6 V, GND = 0 V, T_{OPR} = -40 ºC to +85 ºC

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Serial communication wait time	t_{IF}	-	1	-	-	ms
Temperature sensor data read start time	t_{TSEN}	-	-	-	80	ms
Start-up time	t_{STA}	Output code ±1 °/s	-	-	200	ms

(Note) Conduct serial communication after t_{IF}.
(Note) Conduct temperature sensor data acquisition after t_{TSEN}.
(Note) Conduct angular rate data acquisition after t_{STA}

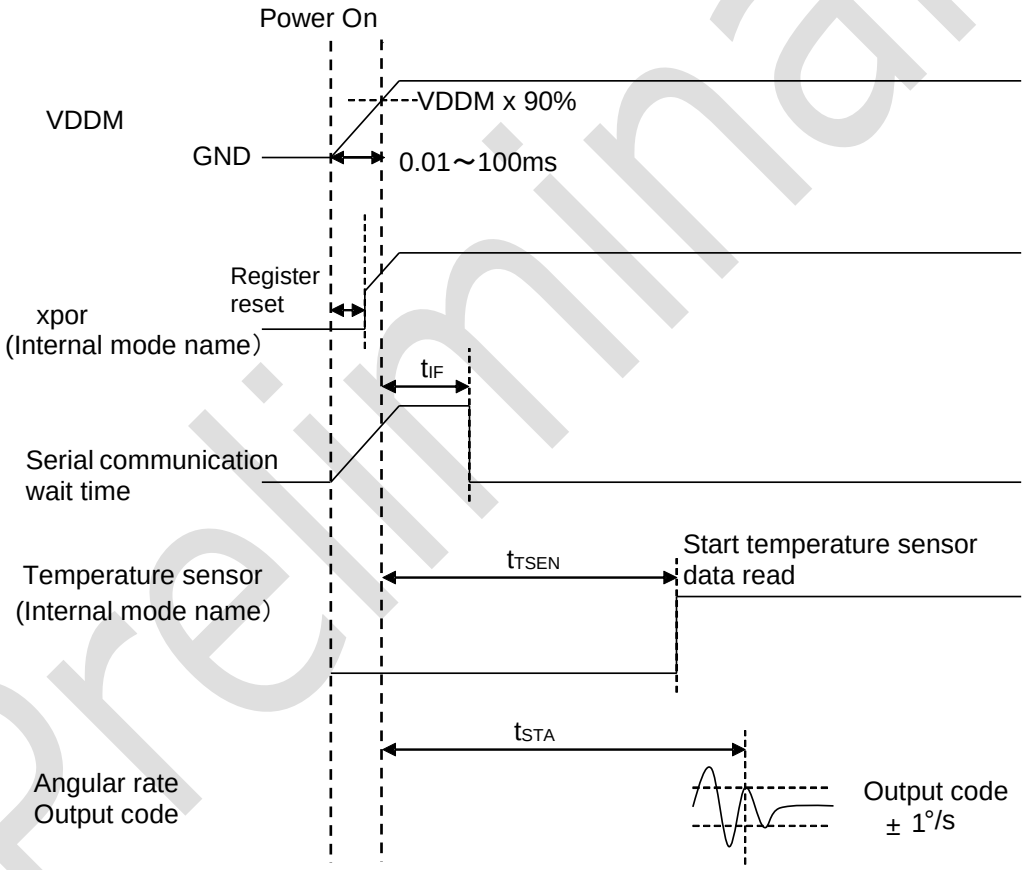


Figure 3.1 Operation Sequence at Start-up

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3.5. Gyro Sensor Characteristics

Table 3.5 Gyro Sensor Characteristics

(V_{DDM} = 2.7 V to 3.6V, V_{DDI} = 1.65 V to 3.6 V, GND = 0 V, T_{OPR} = -40 °C to +85 °C)

Parameter	Symbol	Condition	Min.	Type.	Max.	Unit
Drive frequency	F_d	Frequency code J	50.450	51.025	51.600	kHz
Detuning frequency	D_f		0.7	0.9	1.1	kHz
Scale factor	S_o	16bit, FS = 1x setting		264	-	LSB/(°/s)
		16bit, FS = 4x setting		66	-	
		24bit, FS = 1x setting		67584		
		24bit, FS = 4x setting		16896		
Scale factor tolerance	S_p	T_a = +25 °C	-2	-	+2	%
	S_p	T_a = +25 °C The value includes after the shipment.	-4	-	+4	%
Scale factor variation over temperature	S_{pt}	V_{DDM} = 3 V, T_a=25 °C reference	-3	-	+3	%
Bias	ZRL	T_a = +25 °C	-	0	-	LSB
Bias tolerance	ZRL	T_a = +25 °C	-1	-	+1	°/s
	ZRL	T_a = +25 °C The value includes after the shipment.	-2	-	+2	°/s
Bias variation over temperature	ZRL	V_{DDM} = 3 V, T_a = +25 °C refarence	-1	-	+1	°/s
Rate renge	I	FS = 1x setting	-115		+115	°/s
		FS = 4x setting	-460		+460	
Non-linearity	IN		-0.25	-	+0.25	%FS
Cross-axis sensitivity	CS	T_a = +25 °C	-5	-	+5	%
Current consumption	I_{op1}		-	1150	1400	µA
Sleep current	I_{op3}		-	1	30	µA
Noise density	N_d		-	0.0015	-	(°/s)/√Hz

3.6. Temperature Sensor Characteristics

Table 3.6 Temperature Sensor Characteristics

(V_{DDM} = 2.7 V to 3.6V, V_{DDI} = 1.65 V to 3.6 V, GND = 0 V, T_{OPR} = -40 °C to +85 °C)

Parameter	Symbol	Condition	Min.	Type.	Max.	Unit
Output code	T_{out}	Format 1: Ta = + 25 °C	2560	3200	3840	LSB
		Format 2: Ta = + 25 °C	-1280	0	1280	
temperature error	T_{acc}	T_a = +25 °C	-5	-	+5	°C
Temperature coefficient	T_{its}	Format 1: Ta = + 25 °C	115.2	128	140.8	LSB/°C
		Format 2: Ta = + 25 °C	230.4	256	281.6	

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4. Dimensions and Pin Description

4.1. Outline Dimensions

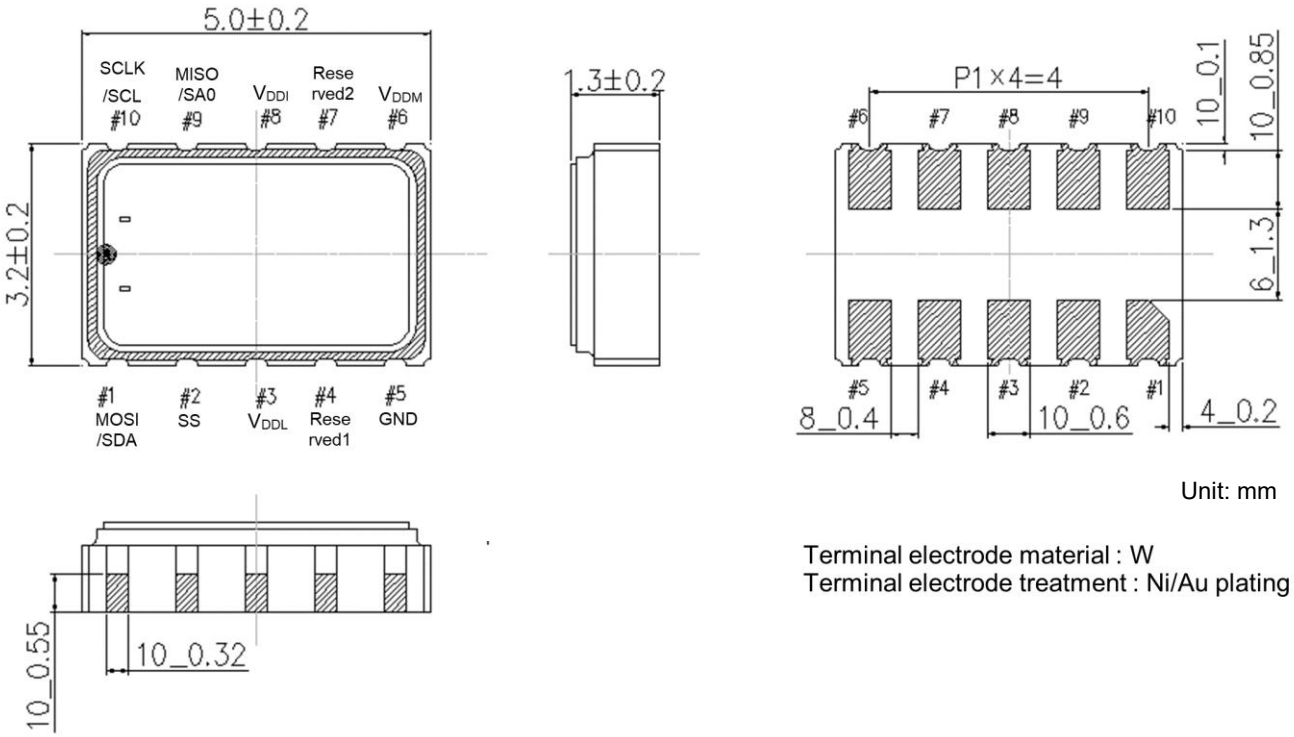


Figure 4.1 Outline Dimensions

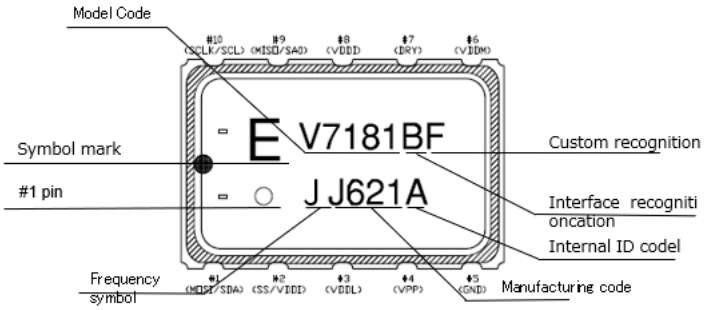
4.2. Pin Name and Description

Table 4.1 Pin Name and Description

Pin number.	Pin name	Input/Output	Pin description
#1	MOSI	Input/Output	4-wire SPI communications mode: serial data input
#2	SS	Input	4-wire SPI communications mode: slave select
#3	V_{DDL}	Output	Internal regulator voltage output Connect to the bypass capacitor 1µF.
#4	Reserved1	Input	Connect to GND.
#5	GND	-	GND
#6	V_{DDM}	-	Power supply voltage
#7	Reserved2	Output	Logic "L" level output Do not connect.
#8	V_{DDI}	-	Power supply voltage for digital interface
#9	MISO	Input/Output	4-wire SPI communications mode: serial data output
#10	SCLK	Input	Serial clock

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4.3. Marking Description



Frequency symbol	Drive frequency
J	**51.000 kHz *)**

Figure 4.2 Marking Discripiton

4.4. Pin Equivalent Circuits

An equivalent circuit for SS, SCLK, MOSI, MISO and Reserved2 is shown in Figure 4.3.

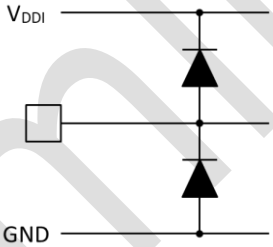


Figure 4.3 The Equivalent Circuit: SS, SCLK, MISO and Reserved2

An equivalent circuit for V_{DDL} and Reserved1 is shown in Figure 4.4.

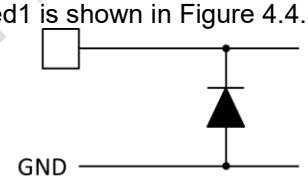


Figure 4.4 The Equivalent Circuit: V_{DDL} and Reserved1

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An equivalent circuit for V_{DDM} and V_{DDI} is shown in Figure 4.5.

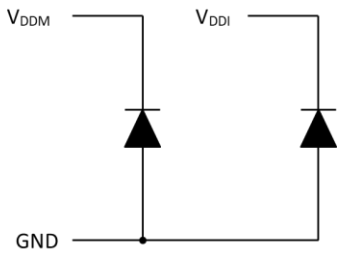


Figure 4.5 The Equivalent Circuit: V_{DDM} and V_{DDI}

4.5. Soldering Pattern

An example of a recommended soldering pattern for this product is shown in During actual board design, give due consideration to design aspects such as mounting density and solder mount reliability to ensure optimal desig

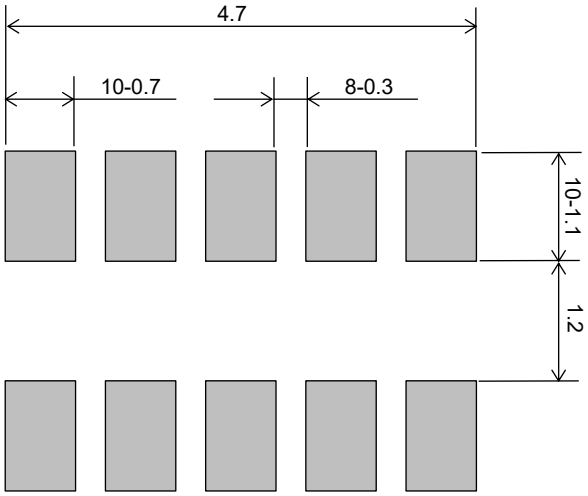


Figure 4.6 Recommended Foot Pattern

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5 Typical Performance Characteristics

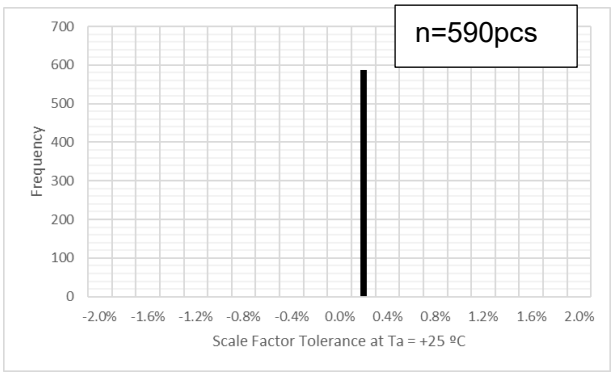


Figure 5.1 Scale Factor Tolerance at T_a = +25 ºC

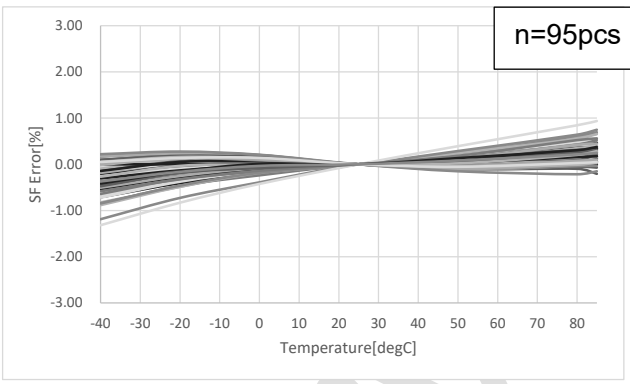


Figure 5.2 Scale Factor Variation over Temperature

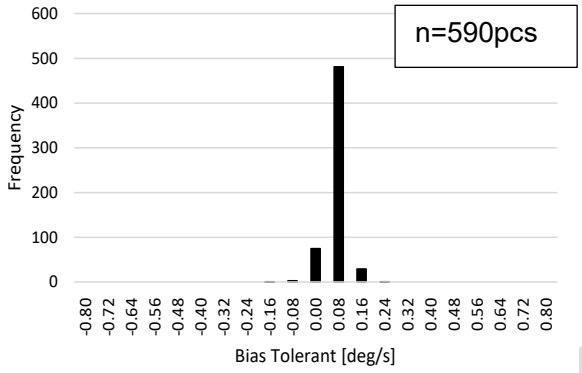


Figure 5.3 Bias Tolerance at T_a = +25 ºC

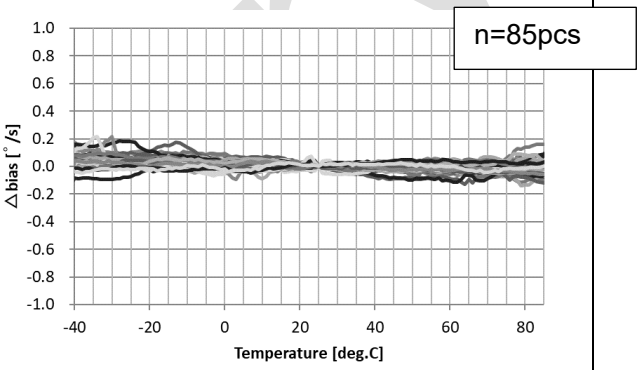


Figure 5.4 Bias Variation over Temperature

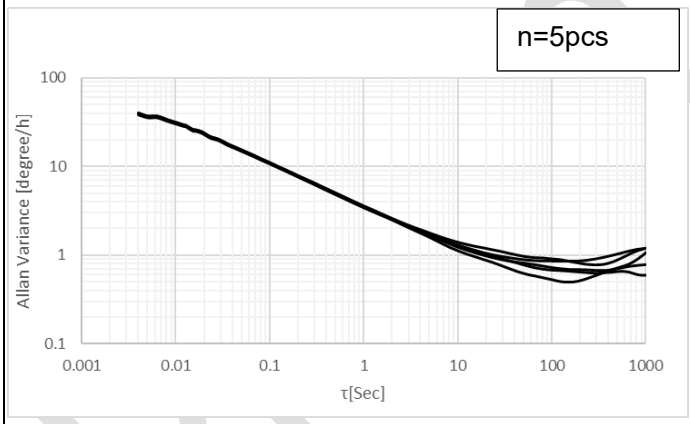


Figure 5.5 Allan Deviation

6 Serial Interface

Access to the sensor is accomplished via serial communication.

4-wire SPI communication is enabled by turning on the power supply V_{DDM}, waiting for the serial communication wait time t_{IF} noted in Section 3.4 to elapse, and then setting the slave select (SS) to logic level "L".

6.1. 4-wire SPI

4-wire SPI communication is 8 bits width serial communication based on the SS, clock signal (SCLK), data input signal (MOSI), and data output signal (MISO)..

With falling edge of SS, the initial byte becomes the address. During serial data transfer, the SS must be maintained at logic level "L." If the SS is set to logic level "H," the serial data transfer will be canceled.

The initial address bit (MSB) is the write/read control bit. Set as "0" to write data to the register and set as "1" to read data from the register.

The subsequent bits 2 (A [6:5]) are set to 2'b01.

Bits 5 (A <4:0>) on the LSB side of the address are the register address. Set the address of the register you want to access. The 2nd byte is the settings value for each register. Refer to the register map in Chapter 6 and transfer the values you want to set.

The register write sequence for 4-wire SPI is shown in Figure 6.1. Write data is transferred after the address. Maintain the SS at logic level "L" during the period between address and data transfer. During the write sequence, the MISO logic level is "L". X is "1" or "0".

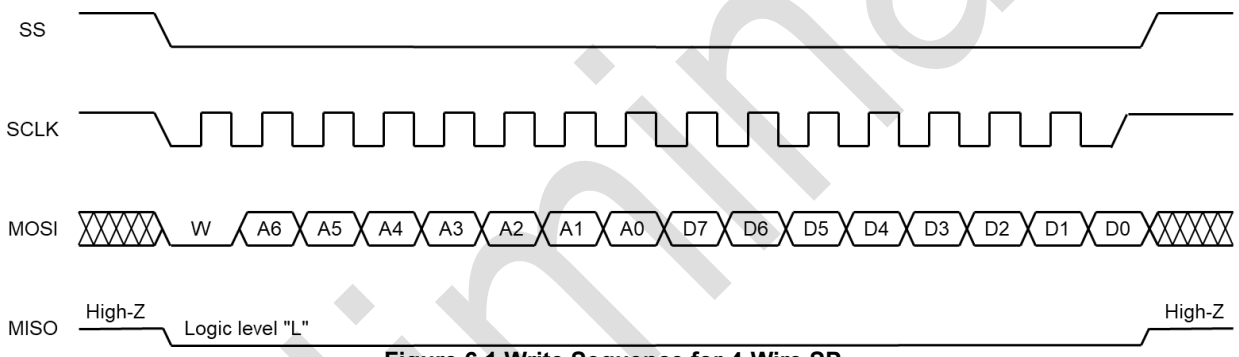


Figure 6.1 Write Sequence for 4-Wire SP

Preliminary

The register read sequence for 4-wire SPI is shown in Figure 6.2. After the address transfer is complete, data will simultaneously output with the SCLK falling edge beginning with the 2nd byte. Similar to the write sequence, during data non-output, the MISO logic level is "L". X is "1" or "0". Angular rate data reads are based on 16 bits output (or 24 bits output based on the angular rate data format selection indicated in Section 7.6). After reading the angular rate data from the 1st byte, maintain logic level "L" for the SS and continue clock input via the SCLK until the desired bit is read (the same applies to reading the temperature sensor data).

The sequence for only the address transfer (command) is shown in Figure 6.3. The register map indicated in Chapter 7 includes the items for only a partial address transfer (command). Similar to the register write sequence, set the first bit (MSB) of the address to "0". Bits 5 (A <4:0>) on the LSB side of the address are the register address (command). Set the address (command) you want to execute. After transferring the address (command), set the SS from logic level "L" to logic level "H" and end the serial communication. During the address tranfer sequence, the MISO logic level is "L". X is "1" or "0".

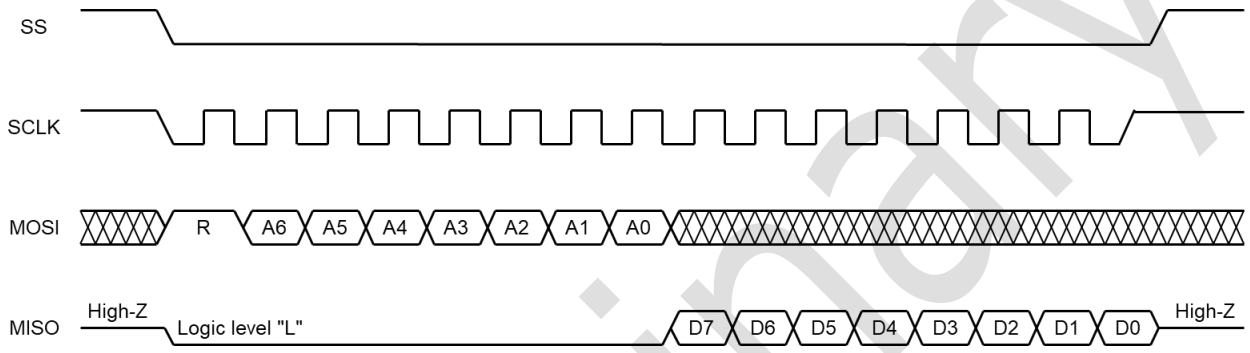


Figure 6.2 Read Sequence for 4-Wire SP

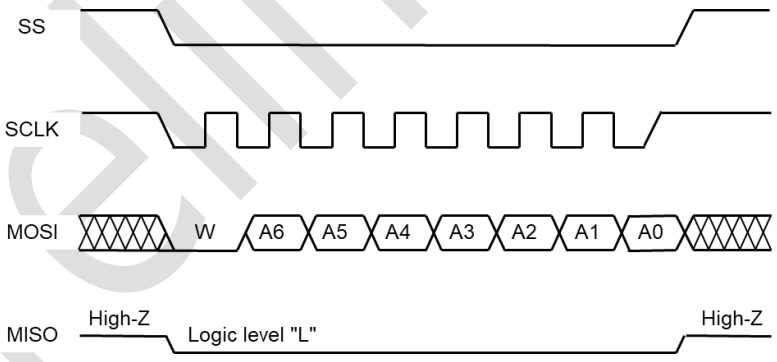


Figure 6.3 Adress Setting Sequence for 4-wire SPI

Preliminary

The timing diagrams for 4-wire SPI are indicated in Figure 6.4 and Figure 6.5.

Table 6.1 AC Characteristics for 4-Wire SPI

(IN_{DDM} = 2.7 V ~ 3.6 V, GND = 0 V, T_{OPR} = -40 °C ~ +85 °C)

Parameter	Symbol	Condition	$V_{DDI} \leq 2.4$ V			$V_{DDI} > 2.4$ V			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
SS setup time	t_{SSS}		15	-	-	15	-	-	ns
SS hold time	t_{SSH}		100	-	-	100	-	-	ns
SS high pulse width	t_{SSHW}		30	-	-	30	-	-	ns
Clock cycle	t_{SCYC}		200	-	-	100	-	-	ns
Clock high pulse width	t_{SHW}		90	-	-	40	-	-	ns
Clock low pulse width	t_{SLW}		90	-	-	40	-	-	ns
Data setup time	t_{SDS}		10	-	-	10	-	-	ns
Dat a hold time	t_{SDH}		10	-	-	10	-	-	ns
Read access time	t_{SACC}	Max. C_L = 30 pF	-	-	80	-	-	30	ns
Output disable time	t_{SOH}		-	-	30	-	-	30	ns

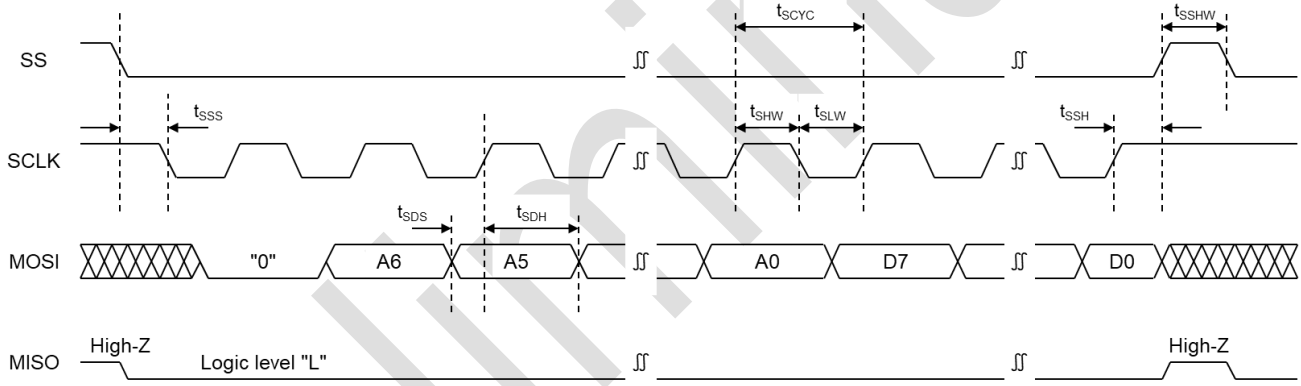


Figure 6.4 Timing Diagram of Writing for 4-Wire SPI

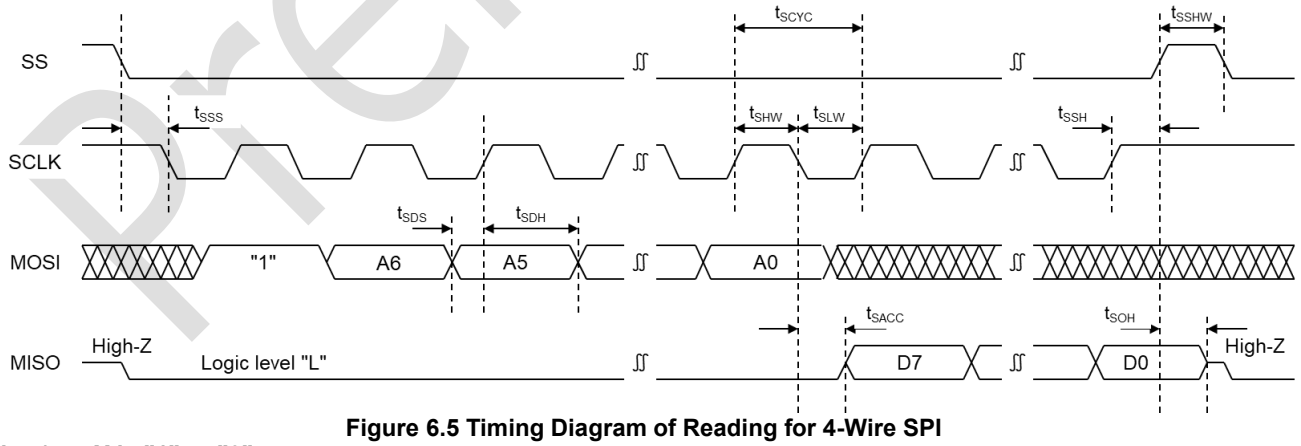


Figure 6.5 Timing Diagram of Reading for 4-Wire SPI

(Note) X is "1" or "0".

Preliminary

6.2. 3-wire SPI

The 3-wire SPI communication is 8 bits width serial communication based on the slave select signal (SS), the clock signal (SCLK), and the data input/output signal (MOSI). Set **SPISel** (register for selecting 3-wire SPI or 4-wire SPI) indicated in1 to "1" (the default value is "0" : 4-wire SPI). Setting **SPISel** to "1" will disable the I^2C communication.

Like 4-wire SPI, with the falling edge of SS the initial byte becomes the address. During serial data transfer, the SS must be maintained at logic level "L". If the SS is set to logic level "H", the serial data transfer will be canceled.

The initial address bit (MSB) is the write/read control bit. Set as "0" to write data to the register and set as "1" to read data from the register. Bits 5 (A <4:0>) on the LSB side of the address is the register address. Set the address of the register you want to access. The 2nd byte is the settings value for each register. Refer to the register map in Chapter 7 and transfer the values you want to set.

The register write sequence for 3-wire SPI is shown in Figure 6.6. Write data is transferred after the address. Maintain the SS at logic level "L" during the period between address and data transfer. X is "1" or "0."

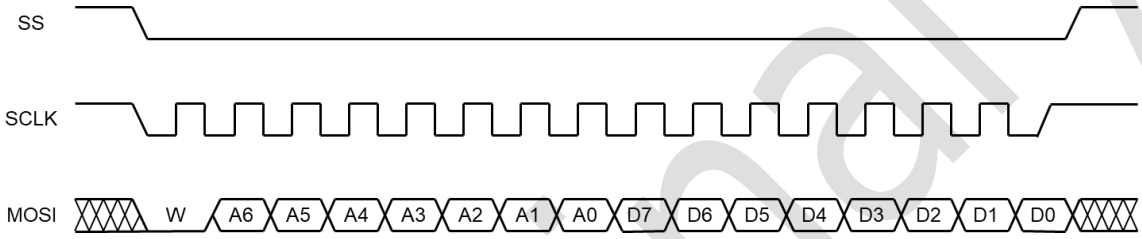


Figure 6.6 Write Sequence for 3-Wire SPI

The register read sequence for 3-wire SPI is shown in Figure 6.7. After the address transfer is complete, data is simultaneously outputted with the SCLK fall beginning from the 2nd byte. Angular rate data reads are based on 16 bits output (or 24 bits output based on the angular rate data format selection indicated in Section 7.6). After reading the angular rate data from the 1st byte, maintain the SS at logic level "L" and continue clock input via the SCLK until the desired bit is read. The same applies to read the temperature sensor data. X is "1" or "0".

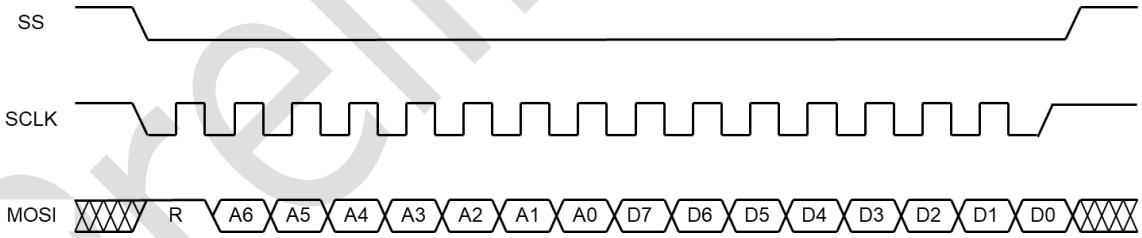


Figure 6.7 Read Sequence for 3-Wire SPI

The sequence for only the address transfer (command) is shown in Figure 6.8. The register map indicated in Chapter 7 includes the items for only a partial address transfer (command). Similar to the register write sequence, set the first bit (MSB) of the address to "0." Bits 5 (A<4:0>) on the LSB side of the address are the register address (command). Set the address (command) you want to execute. After transferring the address (command), set the SS from logic level "L" to logic level "H" and end the serial communication. X is "1" or "0."

The timing diagrams for 3-wire SPI are indicated in Figure 6.9 and Figure 6.10.

Preliminary

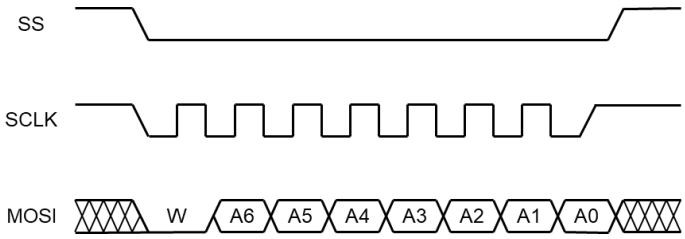


Figure 6.8 Address Setting Sequence for 3-Wire SPI

Table 6.2 AC Characteristics for 3-Wire SPI

V_{DDM} = 2.7 V to 3.6 V, GND = 0 V, T_{OPR} = -20 ºC to +80 ºC

Paramter	Symbol	Condition	$V_{DDI} \leq 2.4$ V			$V_{DDI} > 2.4$ V			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
SS setup time	t_{SSS}		15	-	-	15	-	-	ns
SS hold time	t_{SSH}		100	-	-	100	-	-	ns
SS high pulse width	t_{SSHW}		30	-	-	30	-	-	ns
Clock cycle	t_{SCYC}		200	-	-	100	-	-	ns
Clock high pulse width	t_{SHW}		90	-	-	40	-	-	ns
Clock low pulse width	t_{SLW}		90	-	-	40	-	-	ns
Data setup time	t_{SDS}		10	-	-	10	-	-	ns
Data hold time	t_{SDH}		10	-	-	10	-	-	ns
Read access time	t_{SACC}	Max. C_L = 30 pF	-	-	80	-	-	80	ns
Output disable time	t_{SOH}		-	-	30	-	-	30	ns

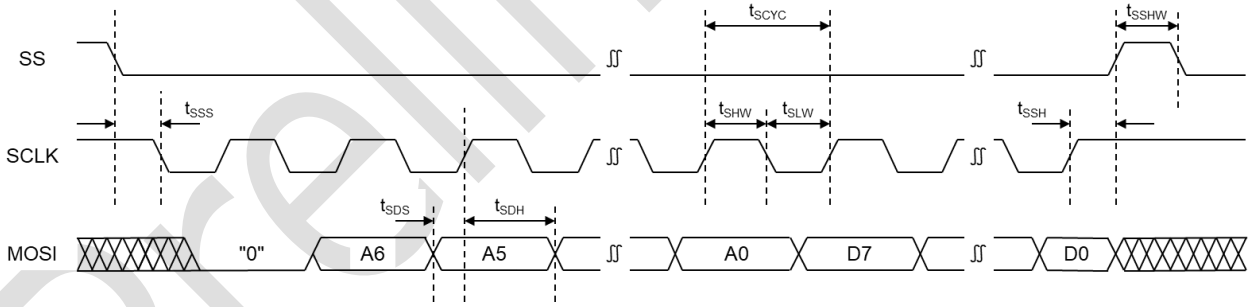


Figure 6.9 Timing Diagram of Writing for 3-Wire SPI

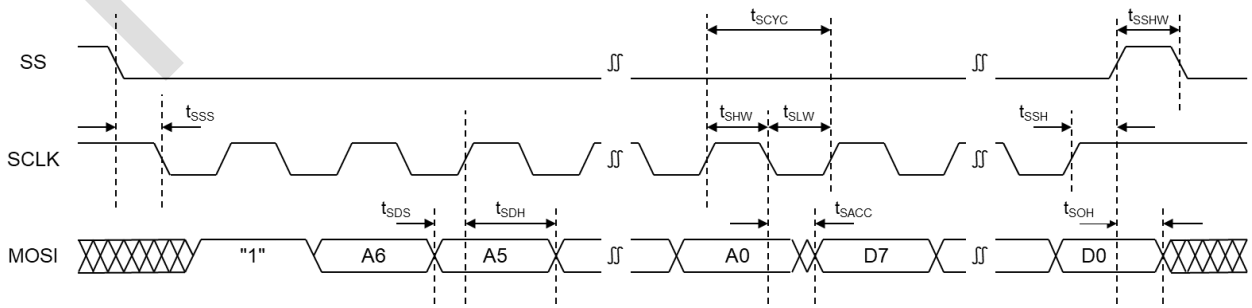


Figure 6.10 Timing Diagram of Reading for 3-Wire SPI

(Note) X is "1" or "0".

Preliminary

6.3. I²C

I²C communication is 8 bits width serial communication based on the clock signal (SCL) and data address signal (SDA). Set **I²C_EN** (register enabling for I²C) indicated in 7.12) to "1" (the default value is "1" : Enable). To use I²C communication, fix the slave select signal (SS) used in 4-wire or 3-wire SPI communication to logic level "H" (interface power supply voltage V_{DDI}).

I²C communication is initiated by issuing the start condition (ST, with SCL status at logic level "H", SDA is changed from logic level "H" to logic level "L") from the master. Or, communication is stopped by issuing the stop condition (SP, with SCL status at logic level "H", SDA is changed from logic level "L" to logic level "H") from the master.
To access the internal register, read (Read = ”1”) /write (Write = ”0”) the slave device address (ADR, address that adds the SA0 "0" or "1" to "110101") to/from the master and transmit the total 1 byte that includes 1 bit ID signal. After ADR receipt, the slave will check to see if the address matches its own address. If matching, the slave returns an ACK (acknowledge), after which communication is possible. If the address does not match, the slave returns to idle mode and waits until another ST is issued.

Internally, the SA0 terminal is set to pull down (approx. 100 kΩ). If the SA0 terminal is set to "0," then connect to N.C. or GND. Or, if the SA0 terminal is set to "1", then connect to V_{DDI}. In this case, a current of approximately 30 µA @ V_{DDI} = 3 V will flow to the SA0 terminal. To reduce the current, add a desired resistor to the V_{DDI} and the SA0 terminal. Alternatively, you can change the terminal setting from pull down to pull up by rewriting the **SelMISO** [1:0] indicated in 7.11 after turning the power ON and once the serial communication wait time t_{IF} indicated in Section 3.4 has elapsed. Refer to 7.11. The MISO/SA0 Pin Control Methods for details on control methods.

Next, send the internal register address (SUB-ADR). Input "0" for the first bit (MSB) of the address (there is not function allocation). The remaining LSB-side 7 bits (A <6:0> are the register address (for detail, refer to register map in Chapter 7). After transferring the addres of the register you wish to access, return an ACK.

The following sequence differs between register write, register read, and address (command) transfer. Please refer to the sequences in Figure 6.11 through Figure 6.13.

Angular rate data reads are based on 16 bits output (or 24 bits output based on the angular rate data format selection indicated in Section 7.6). After reading the angular rate data from the 1st byte, set the master to return an ACK (acknowledge) instead of a NACK (non-acknowledge) and then read the 2nd byte or the 3rd byte. The same applies to read the temperature sensor data.

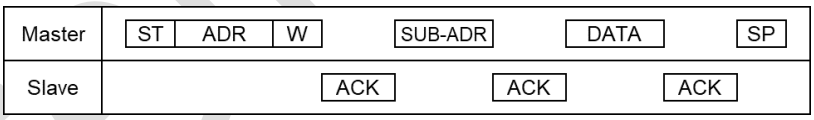


Figure 6.11 Write Protocol for I²C

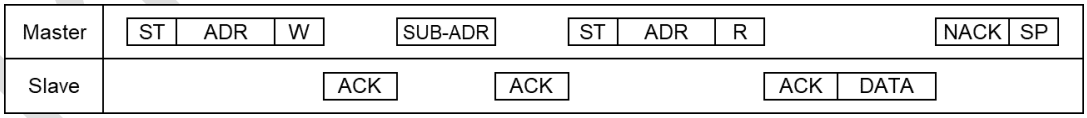


Figure 6.12 Read Protocol for I²C

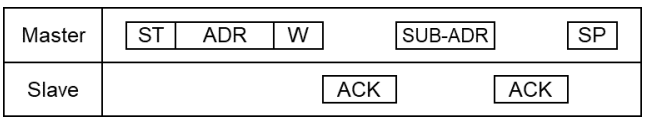


Figure 6.13 Address Setting Protocol for I²C

ST : Start condition
SP : Stop condition
ADR : Slave device address (110101 + SA0)
R/W : Read = “1”, Write = “0”
SUB-ADR : Internal register address
DATA : Internal register read/write data
ACK : “Low”
NACK : “High”, send at read complete.

As an example of a waveform, register write, register read, and address setting sequence are shown in Figure 6.14 through Figure 6.16.

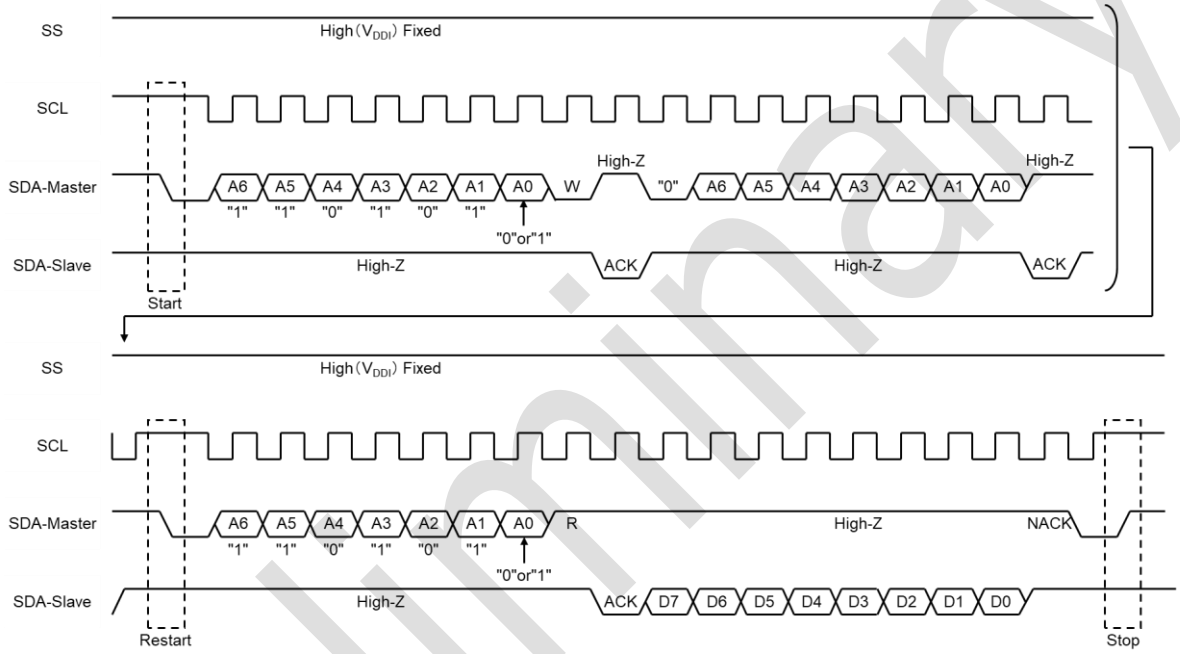


Figure 6.14 Write Sequence for I²C

Preliminary

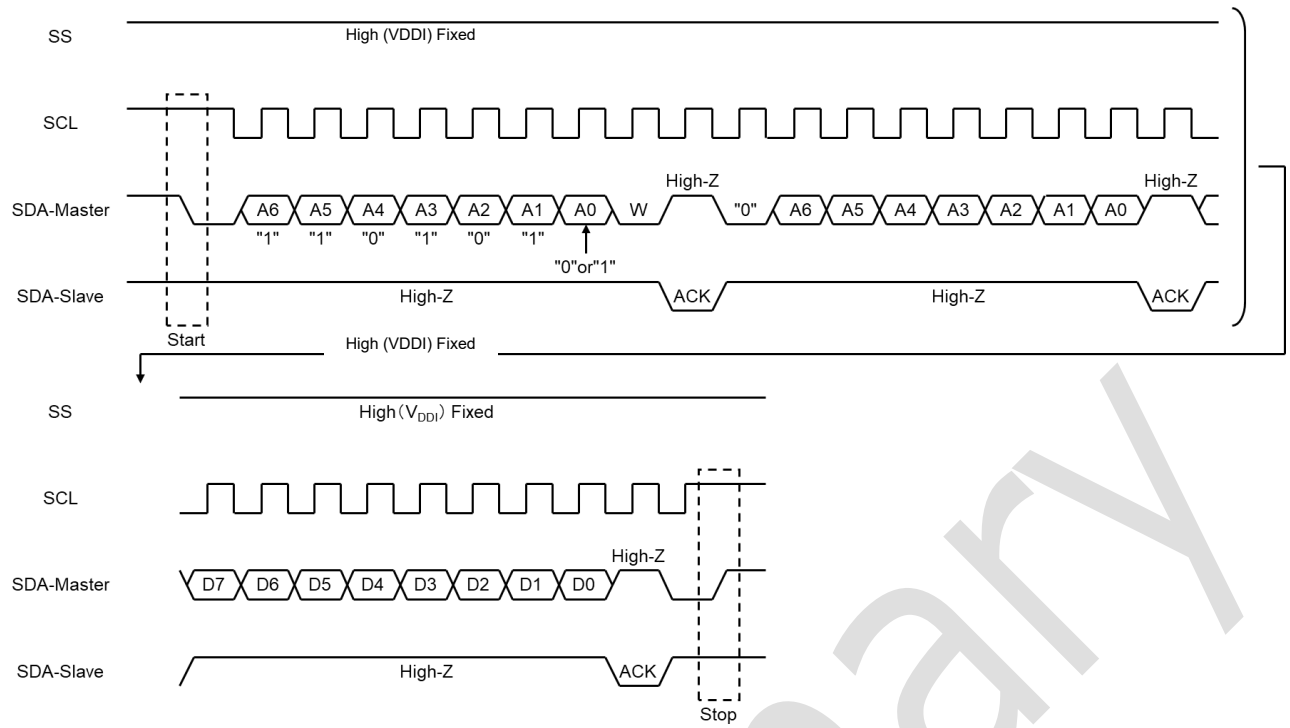


Figure 6.15 Read Sequence for I²C

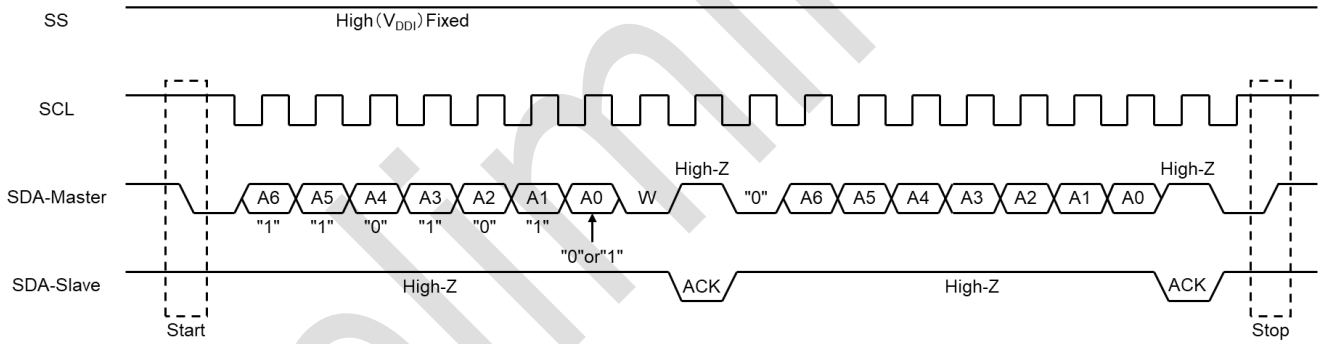


Figure 6.16 Address Setting Sequence for I²C

Preliminary

6.4. Angular Rate Data Read

6.4.1. 4-Wire SPI, 3-Wire SPI, I²C

The angular rate read function is conducted using the **DatAccOn** indicated in Table 7.1. Angular rate data uses the 2's compliment expression and has a data width of 16 bits or 24 bits (switch using the **DataFormat** indicated in Table 7.5). During serial communication, after reading the angular rate data from the 1st byte, maintain logic level "L" for the SS and continue clock input via the SCLK until the desired bit is read.

Table 6.3 Angular Rate Data Output Control

A [6:5]	**DataFormat**	Data output order		
		1st byte	2nd byte	3rd byte
00	0	D [15:8]	D [7:0]	
00	1	D [23:16]	D [15:8]	D [7:0]

(Note) **DataFormat** is the angular rate data format indicated in Table 7.5

When in 4-wire SPI or 3-wire SPI communication mode, after reading the angular rate data from the 1st byte, maintain logic level "L" for the SS and continue clock input via the SCLK until the desired bit is read.

When in I²C communication mode, after reading the angular rate data from the 1st byte, set the master to return an ACK (acknowledge) instead of a NACK (non-acknowledge) and then read the 2nd byte or the 3rd byte.

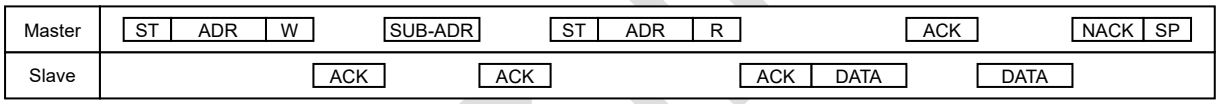


Figure 6.17 Angular Rate Data (16 Bits Output)

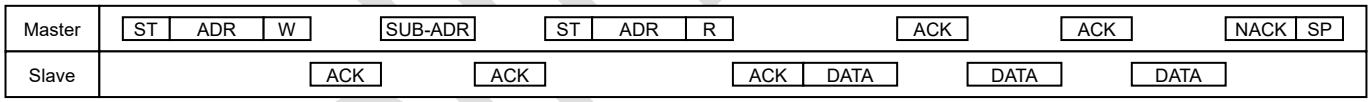


Figure 6.18 Angular Rate Data (24 Bits Output)

Preliminary

6.5. Temperature Data Read

The temperature sensor data read is conducted using the TempRd indicated in Table 7.1. The temperature sensor data uses the 2's complement expression and has a data width of 16 bits. And you can select from the types by writing the "TFormat" in the address 0x0b of the Table 7.1. For reading, just like reading angular rate data, continue serial communication until any bit is read. Note that temperature sensor data is updated at sampling rate.

Table 6.4 Temperature Sensor Data Output Control

TFormat	Temperature Sensor Output	
	Sensitivity	0 Cord Temperature
0	128LSB/ degC	0 degC
1	256LSB/ degC	25 degC

6.6. Command Validation Time

6.6.1. 4-Wire SPI, 3-Wire SPI

Table 6.5 Restriction Time for Command Issuance in SPI Communication

(IN_{DDM} = 2.7 V~ 3.6 V, GND = 0 V, T_{OPR} = -40 degC ~ +85 degC)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Sleep-in wait time	t_{SLPIN}	10	-	-	µs
Sleep-out wait time (Note 1)	t_{SLPOUT}	10	-	-	µs
Standby wait time	t_{STBY}	10	-	-	µs
Software reset wait time	t_{SWRST}	10	-	-	µs

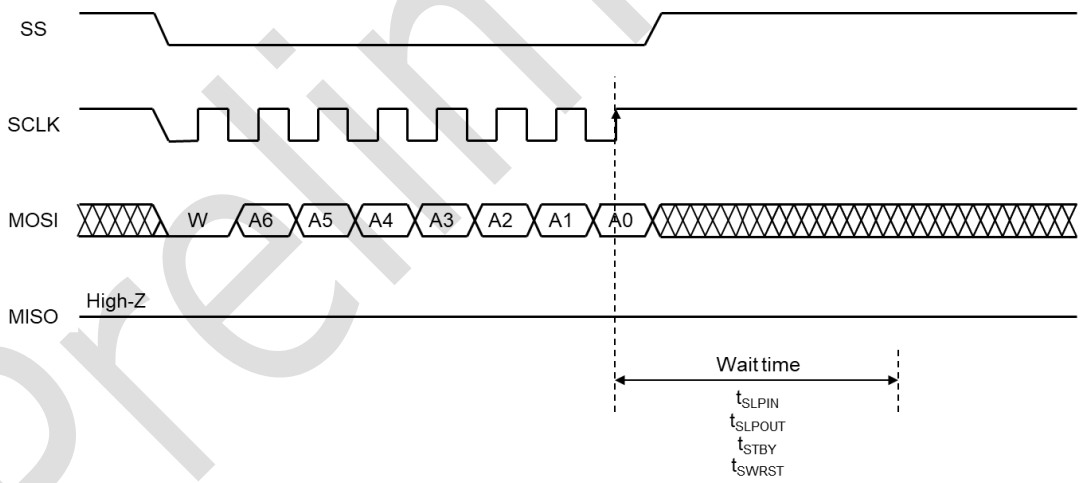


Figure 6.19 Command Validation Tme for SPI

(Note 1) Sleep-out command is validated after Sleep-in or Standby command issued and wait for t_{SLPOUT} or t_{STBY} to elapse.
(Note) X is "1" or "0".

Preliminary

6.6.2. I²C

Table 6.6 Command Validation Time for I²C

V_{DDM} = 2.7 to 3.6 V, GND = 0 V, T_{OPR} = -20 ºC to +80 ºC

Parameter	Symbol	Min.	Typ.	Max.	Unit
Sleep-in wait time	t_{SLPIN}	10	-	-	µs
Sleep-out wait time (Note 1)	t_{SLPOUT}	10	-	-	µs
Standby wait time	t_{STBY}	10	-	-	µs
Software reset wait time	t_{SWRST}	10	-	-	µs

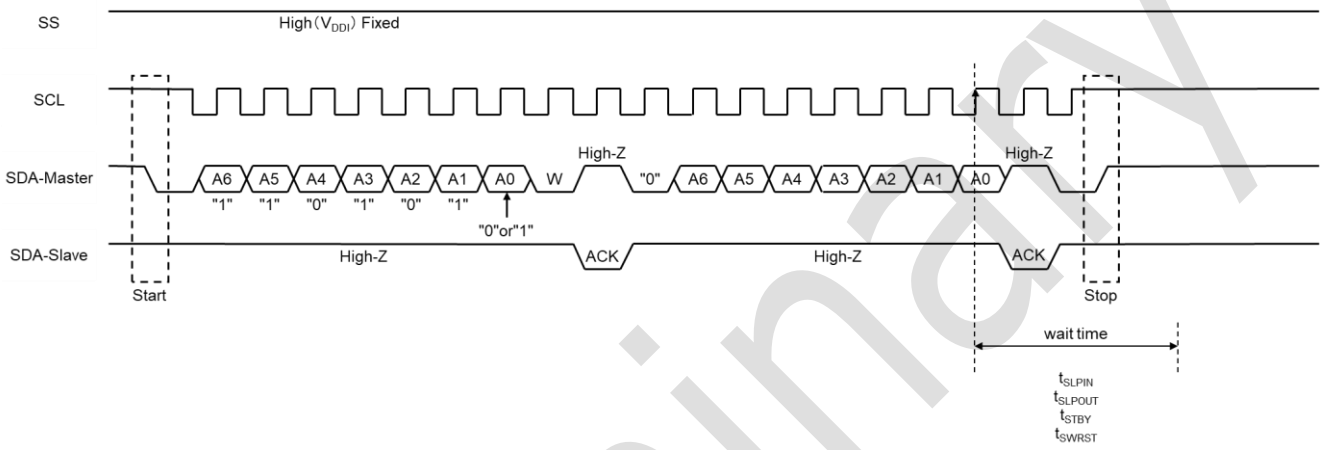


Figure 6.20 Command Validation Time for I²C

(Note 1) Sleep-out command is validated after Sleep-in or Standby command issued and wait for t_{SLPOUT} or t_{STBY} to elapse.

Preliminary

7 User Command Register

Table 7.1 User Command Register

Address	Register	R/W	Function
0x00	Reserved		
0x01	DspCtl1	R/W	DSP settings 1
0x02	DspCtl2	R/W	DSP settings 2
0x03	Reserved		
0x04	StsRd	R	Status read
0x05	Status	R/W	Sleep-in
0x06	ProtState	R/W	Sleep-in control
0x07	Reserved		
0x08	TempRd	R	Temperature sensor data read
0x09	Reserved		
0x0a	DatAccOn	R	Angular rate data read
0x0b	OutCtl1	R/W	Angular rate data read control
0x0c	SelFSR	R/W	Full scale range switching
0x0d	DspRes	R/W	Digital filter reset
0x0e	Reserved		
0x0f	Reserved		
0x10	Reserved		
0x11	Reserved		
0x12	Reserved		
0x13	Reserved		
0x14	Reserved		
0x15	DatLatchCom	R/W	Command data latch
0x16	Reserved		
0x17	Reserved		
0x18	Reserved		
0x19	Reserved		
0x1a	ProtSoftR	R/W	Software reset control
0x1b	SoftReset	R/W	Software reset
0x1c	Reserved		
0x1d	OtCtl	R/W	MISO control
0x1e	Reserved		
0x1f	IFCtl	R/W	Serial interface settings

R: Register read

R / W: Register read and register write

(Note) Reserved resister must not be changed. Writing to those registers may cause permanent damage to the device..

Preliminary

7.1. DSP Setting 1

Table 7.2 DSP Setting 1

address	Bit	registername	initial value	R/W	function	Settings
0x01	7	Reserved	0	R	Reserved	Reserved
	6	Reserved	0	R	Reserved	Reserved
	5	Reserved	0	R	Reserved	Reserved
	4	Reserved	0	R	Reserved	Reserved
	3	Reserved	0	R	Reserved	Reserved
	2	Reserved	0	R	Reserved	Reserved
	1	Reserved	0	R	Reserved	Reserved
	0	RevSign	0	R/W	Reserved	Reserved

(Note 1) When changing the setting, set the initial value except for the change bit. The settings can be changed at the same time if they are in the same register (same address).
(Note 2) Do not change the reserved register and use the default value.
(Note3) RevSign register and do not change it and use it with the default value.

7.2. DSP setting 2

Table 7.3 DSP Setting 2

Address	Bit	Register	Default	R/W	function	Settings
0x02	7	Reserved	0	R	Reserved	Reserved
	6	EnbNF	0	R/IN	Notch filter for the Detune frequency	0：Disable, 1：Enable
	5	LpfOrder[1]	0	R/W	LPF order select	**LpfOrder** [1:0] 00: 2nd 01: 3rd 10: 4th 11：Not Available
	4	LpfOrder[0]	0	R/W		
	3	LpfFc[3]	0	R/W	LPF f_c Select	LpfFc[3:0] 0000：1Hz 0001：10Hz 0010：25Hz 0011：50Hz 0100：100Hz 0101：200Hz 0110：400Hz 0111：500Hz
	2	LpfFc[2]	1	R/W		
	1	LpfFc[1]	0	R/W		
	0	LpfFc[0]	0	R/W		

(Note 1) When changing the setting, set the initial value except for the change bit. If the bits are in the same register (same address), the settings can be changed at the same time.
(Note 2) Do not change the Reserved register and use the default value.

Preliminary

7.3.Status Read

アドレス	ビット	レジスター名	初期値	タイプ	機能	設定内容
0x04	7	Reserved	Reserved	R	Reserved	Reserved
	6	Reserved	Reserved	R	Reserved	Reserved
	5	Reserved	Reserved	R	Reserved	Reserved
	4	Reserved	Reserved	R	Reserved	Reserved
	3	Reserved	Reserved	R	Reserved	Reserved
	2	Reserved	Reserved	R	Reserved	Reserved
	1	Reserved	Reserved	R	Reserved	Reserved
	0	ProcOK	-	R	Temperature sensor Data Output flag	0：Preparing 1：Ready

7.4. Sleep In / Sleep Out Control

Sleep In is the address "0x05" of SlpIn of "0" from "1" It will be executed by. However, the Sleep In is protected. Therefore, before performing a Sleep In, the address "0x06" register "0x59" set to.

During sleep, only register access is possible. Status for angular rate data and temperature sensor data is "0". If you escape the Sleep In, the DSP is initialized.

Table 7.4 Sleep In/ Sleep Out Contorol

Address	Bit	Register	Default	R/W	Function	Settings
0x05	7	Reserved	0	R	Reserved	Reserved
	6	Reserved	0	R	Reserved	Reserved
	5	Reserved	0	R	Reserved	Reserved
	4	Reserved	0	R	Reserved	Reserved
	3	Reserved	0	R	Reserved	Reserved
	2	Reserved	0	R	Reserved	Reserved
	1	Reserved	0	R	Reserved	Reserved
	0	SlpIn	0	R/W	Sleep In Control	0：Sleep Out 1：Sleep In
0x06	7	ProtState[7]	0	R/W	Sleep In control Enable	When 0x59 is written, SipIn is enable.
	6	ProtState[6]	0	R/W		
	5	ProtState[5]	0	R/W		
	4	ProtState[4]	0	R/W		
	3	ProtState[3]	0	R/W		
	2	ProtState[2]	0	R/W		
	1	ProtState[1]	0	R/W		
	0	ProtState[0]	0	R/W		

7.5. Temperature Sensor Data Read

Specify address as "0x08". Only data read (no data write). Refer to Section 6.5 regarding the temperature sensor data read function.

7.6. Angular Rate Data Read

Specify address as "0x0a". Only data read (no data write). Refer to Section 6.4 regarding the angular rate data read function.

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7.7. Angular Rate Data Read Control

Table 7.5 Angular Rate Data Read Control

Address	Bit	Register	Default	R/W	Function	Settings
0x0b	7	EnbImuLatch	0	R/W	Trigger data latch function enabled	0：Disable, 1：Enable
	6	Reserved	0	R/W	Reserved	Reserved
	5	EnbCmdTrg	0	R/W	Command data latch function enabled	0：Disable, 1：Enable
	4	Reserved	0	R/W	Reserved	Reserved
	3	TFormat	0	R/W	Temperature sensor data format	0:16bit(128LSB/ degC） 1:16bit(256LSB/ degC)
	2	DataFormat	0	R/W	Angular velocity data format	0：16bitoutput 1：24bitoutput
	1	OutCtl[1]	0	R/W	Angular velocity data Output selection	OutCtl[1:0] 00: Evaluation mode1(Note2） 01: Angular velocity data output 10: Evaluation mode2(Note2） 11: Evaluation mode3(Note2）
	0	OutCtl[0]	1	R/W		

(Note 1) When changing the setting, set the initial value except for the change bit. If the bits are in the same register (same address), the settings can be changed at the same time.
(Note 2) Do not change the Reserved register and use the default value.

7.8. Full Scale Control

Address" 0x0c"Change the full scale range with the register of ± 115 °/ s(FS=1x setting)、±460°/s(FS=4x setting)Can be set to.

Table 7.6 Full Scale Control

Address	Bit	Register	Default	R/W	function	Settings
0x0c	7	Reserved	0	R	Reserved	Reserved
	6	Reserved	0	R	Reserved	Reserved
	5	Reserved	0	R	Reserved	Reserved
	4	Reserved	0	R	Reserved	Reserved
	3	Reserved	0	R	Reserved	Reserved
	2	Reserved	0	R	Reserved	Reserved
	1	SelFSR[1]	0	R/W	Full scale range switching	00：FS=1x setting 01：Not set 10：FS=4x setting 11：Not set
	0	SelFSR[0]	0	R/W		

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7.9. Data Latch Command Control

The data latch function is a function that can latch the angular velocity data at any timing and read the latch data. The data latch function can be enabled by using the register with the address "0x0b" shown in Table 7.5. The trigger data latch function is enabled by setting “EnbImuLatch” to “1”. Also, the command data latch function is enabled by setting “EnbCmdTrg” to “1”.

It is shown in the normal angular velocity readout timing chart at Figure 7.1. When the data latch function is disabled, the data at the time when the command for reading the angular velocity request is input is output as described in Figure 6.1.

On the other hand, the data latch function latches internal data at any time using a trigger signal or command. Latch data will be read as angular velocity data in the subsequent angular velocity reading. Note that the latched read data will not be updated unless a new latch operation is performed.

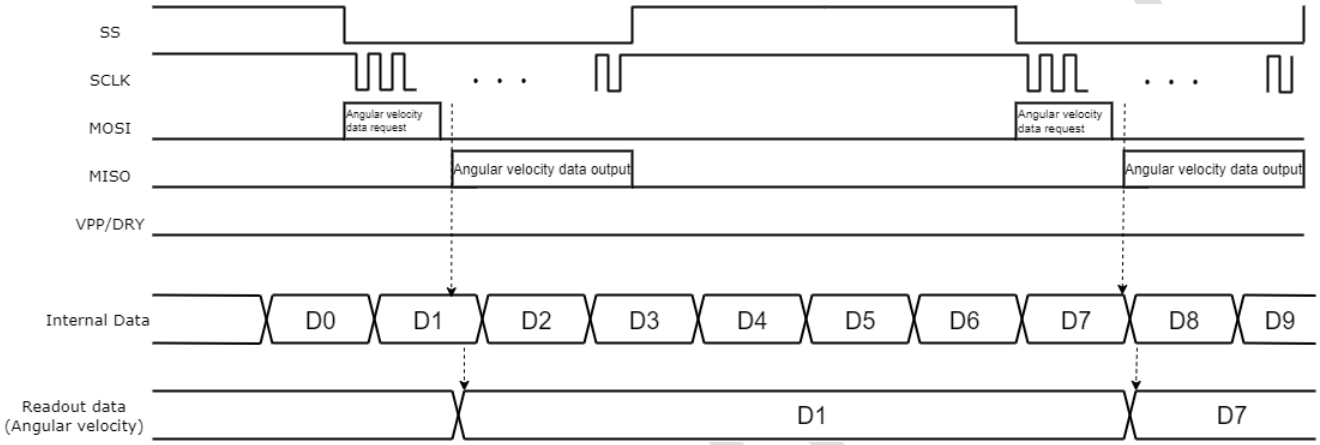


Figure 7.1 Normal Angular Rate read Timing Chart

7.9.1. Trigger Data Latch Function

It is shown the timing chart of the trigger data latch function in the Figure 7.2. When the H pulse trigger signal is input to MOSI during the period of SS = H, the Internal data of the angular velocity data is latched. After the data is latched, the latched data is output when the angular velocity request is input. After that, the read data is not updated unless a new trigger signal is input.

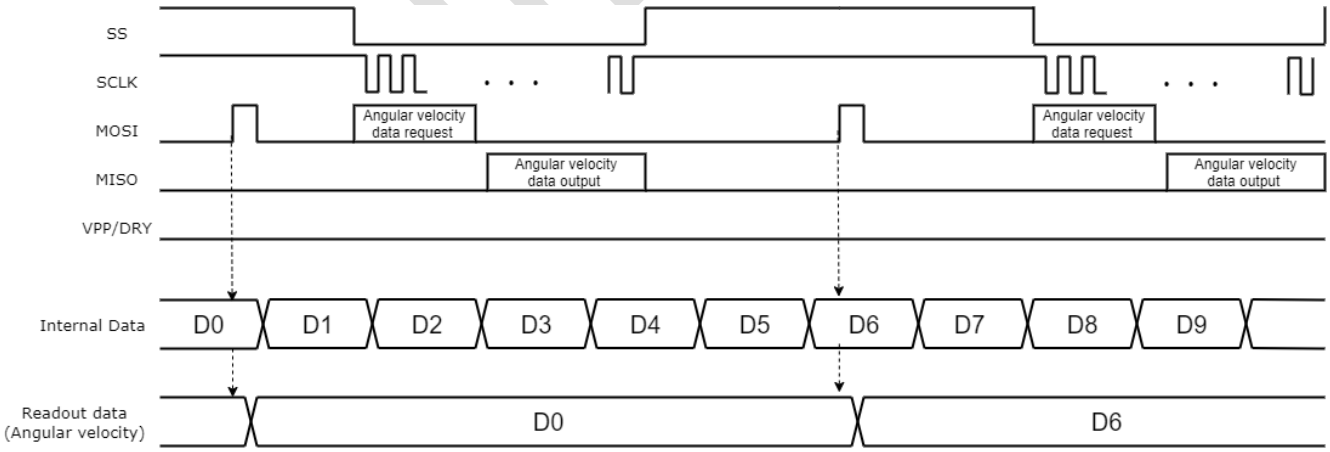


Figure 7.2 Trigger Data Latch Timing Chart

※When you use the MOSI path with other devices, this sensor recognize as the trigger pulse in the communication with other device. So, the angular velocity data is updated. Please be careful when doing so.

7.9.2. Command Data Latch Function

The command data latch function is a function to latch the internal angular rate data by setting DatLatchCom of the address "0x15" in "1"(Table 7.7). After the data is latched, the latched data is output when the angular velocity request is input. After that, the read data will not be updated unless a new latch command is executed. Therefore, if you want to latch the data again, set DatLatchCom to "0" once, and then set DatLatchCom to "1".

Table 7.7 Data Latch Command Control

Address	Bit	Register	Default	R/W	Function	Settings
0x15	7	Reserved	0	R	Reserved	Reserved
	6	Reserved	0	R	Reserved	Reserved
	5	Reserved	0	R	Reserved	Reserved
	4	Reserved	0	R	Reserved	Reserved
	3	Reserved	0	R	Reserved	Reserved
	2	Reserved	0	R	Reserved	Reserved
	1	Reserved	0	R	Reserved	Reserved
	0	DatLatchCom	0	R/W	Command data latch	0→1: Perform data latch

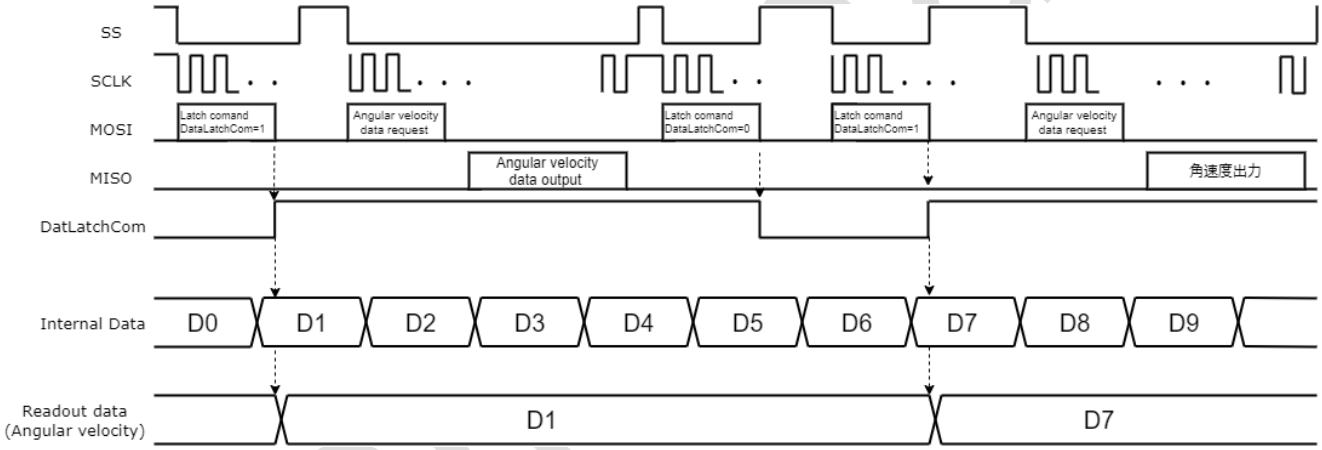


Figure 7.3 Data Command Latch Timing Chart

Preliminary

7.10. Software Reset Control / Software Reset

Software reset is the address "0x1A" of software reset of "0" from "1" It will be executed by. However, the software reset operation is protected. Therefore, before performing a software reset, the address "0x1A" register "0x59" set to.

Table at software reset the user command register shown in 6.1 is initialized (set to the register initial value).

Table 7.8 Software Reset Control

Address	Bit	Register	Default	R/W	Function	Settings
0x1A	7	ProtSoftR[7]	0	R/W	Software reset enable control.	0x59 Soft resetIs valid
	6	ProtSoftR[6]	0	R/W		
	5	ProtSoftR[5]	0	R/W		
	4	ProtSoftR[4]	0	R/W		
	3	ProtSoftR[3]	0	R/W		
	2	ProtSoftR[2]	0	R/W		
	1	ProtSoftR[1]	0	R/W		
	0	ProtSoftR[0]	0	R/W		
0x1B	7	Reserved	0	R	Reserved	Reserved
	6	Reserved	0	R	Reserved	Reserved
	5	Reserved	0	R	Reserved	Reserved
	4	Reserved	0	R	Reserved	Reserved
	3	Reserved	0	R	Reserved	Reserved
	2	Reserved	0	R	Reserved	Reserved
	1	Reserved	0	R	Reserved	Reserved
	0	SoftReset	0	R/W	Software reset	0→1: Software reset execution

7.11. MISO / SA0 Pin Controlol

The MISO / SA0 Pin Controlol is the address "0x1d" in the Table.6.1. The MISO / SA0 Output is changed by writing the "SelMISO[1:0]". The pin condion is shown in the table. 6.10.

Table 7.9 Control of the MISO/SA0 pin

Address	Bit	Register	Default	R/W	Function	Settings
0x1d	7	Reserved	0	R	Reserved	Reserved
	6	Reserved	0	R	Reserved	Reserved
	5	Reserved	0	R	Reserved	Reserved
	4	Reserved	0	R	Reserved	Reserved
	3	Reserved	0	R	Reserved	Reserved
	2	Reserved	0	R	Reserved	Reserved
	1	SelMISO[1]	1	R/W	MISO/SA0 pin Starus select	（Note 3）
	0	SelMISO[0]	0	R/W		

Table 7.10 Condition of the MISO/SA0 Pin Control.

Mode	SPISel	SelMISO[1]	SelMISO[0]	SS	MISO/SA0
4-wire SPI	0（4-wire SPI）	X	X	0	Output
	0	0	0	1	Output "L" level
	0	0	1	1	Output "H" level
	0	1	X	1	High-Z

（Note 1） Initial value is "1" in the SelMISO[1] and it is "0" in the SelMISO[0].

（Note 2） In case of the readings the pin outputs, in the other status it is High-Z.

（Note 3） SA0 is fixed "Low" in the IC intenal.

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7.12. Serial Interface Settings

Table 7.11 Serial Interface Settings

Address	Bit	Register	Default	R/W	Function	Settings
0x1f	7	Reserved	0	R	Reserved	Reserved
	6	Reserved	0	R	Reserved	Reserved
	5	Reserved	0	R	Reserved	Reserved
	4	Reserved	0	R	Reserved	Reserved
	3	Reserved	0	R	Reserved	Reserved
	2	Reserved	0	R	Reserved	Reserved
	1	**SPISel** (Note 1)	0	R/W	4-wire/3-wire SPI select	0: 4-wire SPI, 1: 3-wire SPI
	0	**I²C_EN** (Note 1)	1	R/W	I²C enable	0: Disable, 1: Enable

(Note) The mode indicated in Table 7.11 can be changed only by SPI communication.

(Note) Reserved resister must not be changed. Use the default settings.

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8 Filter Characteristics

8.1. Digital Filter

8.1.1. Selectable digital Low-Pass Finter (LPF)

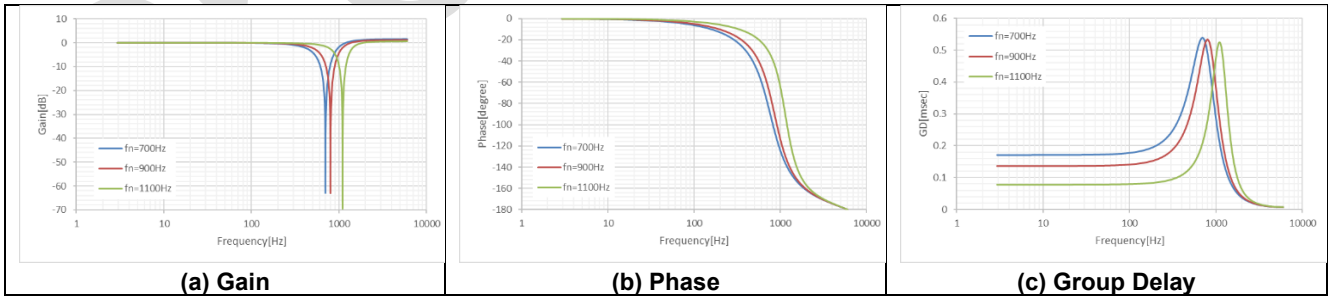
The typical characteristic values of the selectable digital LPF are shown in Table 8.1. The digital LPF has selectable filter orders (2nd, 3rd and 4th order) and cutoff frequencies (1Hz to 500 Hz). See Section 7.2 for the setting instructions.

Table 8.1 Selectable Digital LPF

Parameter	Condition		Type.			Unit
	LpfFc [3:0]	f_c	2nd order	3rd order	4st order	
Phase @ 10 Hz	0000	1 Hz	-164.6	-240.7	-314.1	°
	0001	10 Hz	-65.5	-80.8	-94.0	°
	0010	25 Hz	-28.7	-34.5	-39.3	°
	0011	50 Hz	-14.6	-17.3	-19.8	°
	0100	100 Hz	-7.3	-8.7	-9.9	°
	0101	200 Hz	-3.7	-4.3	-4.9	°
	0110	400 Hz	-1.8	-2.2	-2.5	°
	0111	500 Hz	-1.5	-1.7	-2.0	°
Group delay @ DC	0000	1 Hz	239.7	280.6	318.5	ms
	0001	10 Hz	20.7	24.5	27.9	ms
	0010	25 Hz	8.2	9.8	11.1	ms
	0011	50 Hz	4.1	4.9	5.6	ms
	0100	100 Hz	2.1	2.4	2.8	ms
	0101	200 Hz	1.0	1.2	1.4	ms
	0110	400 Hz	0.5	0.6	0.7	ms
	0111	500 Hz	0.4	0.5	0.6	ms

8.1.2. Notch Filter (NF)

Please refer to Section 12.3 for the setting instructions. For more details on the filter characteristics, please contact us. The center frequency f_n (700 Hz ～ 1100 Hz) of the filter is set at the factory individually, and it cannot be changed. It is possible to select whether enable or disable the Notch Filter. The characteristic of the Notch Filter is shown in the Figure 8.1 and Table 8.2.



(a) Gain (b) Phase (c) Group Delay

Figure 8.1 Bode plots of the Notch Filter (NF)

Table 8.2 Characteristic of the Notch Filter (NF)

Item	Condition f_n	Typ.	Unit
Phase@ 10 Hz	700 Hz	-0.63	°
	900 Hz	-0.50	°
	1100 Hz	-0.29	°
Group Delay@ 10 Hz	700 Hz	0.17	ms
	900 Hz	0.14	ms
	1100 Hz	0.08	ms

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9 Connection Diagram

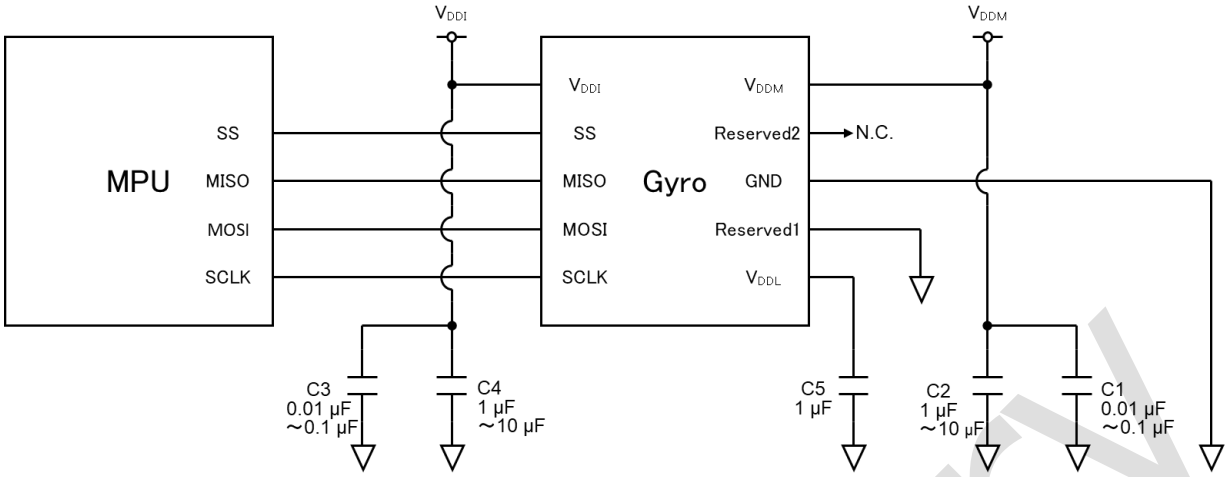


Figure 9.1 Example of 4-Wire SPI Connection

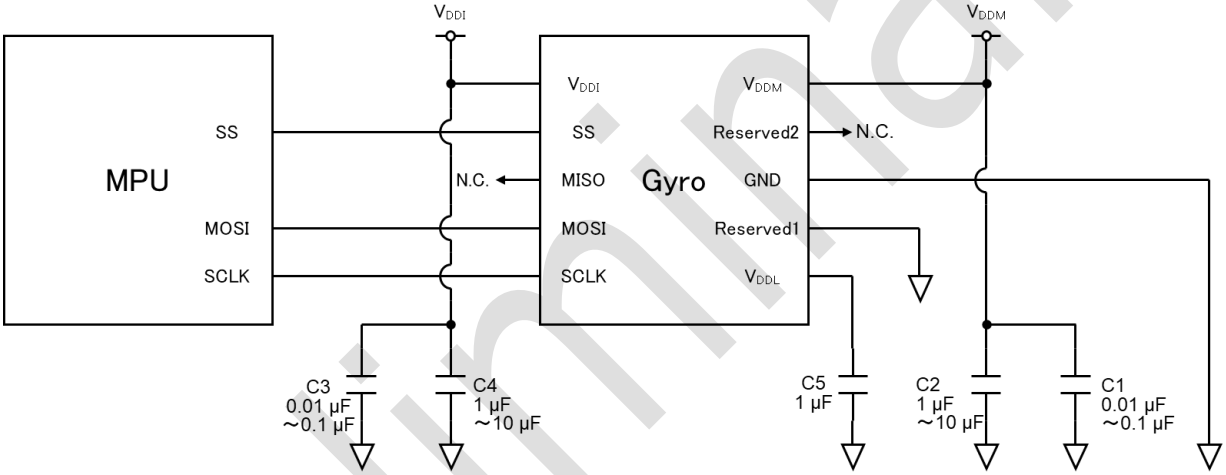


Figure 9.2 Example of 3-Wire SPI Connection

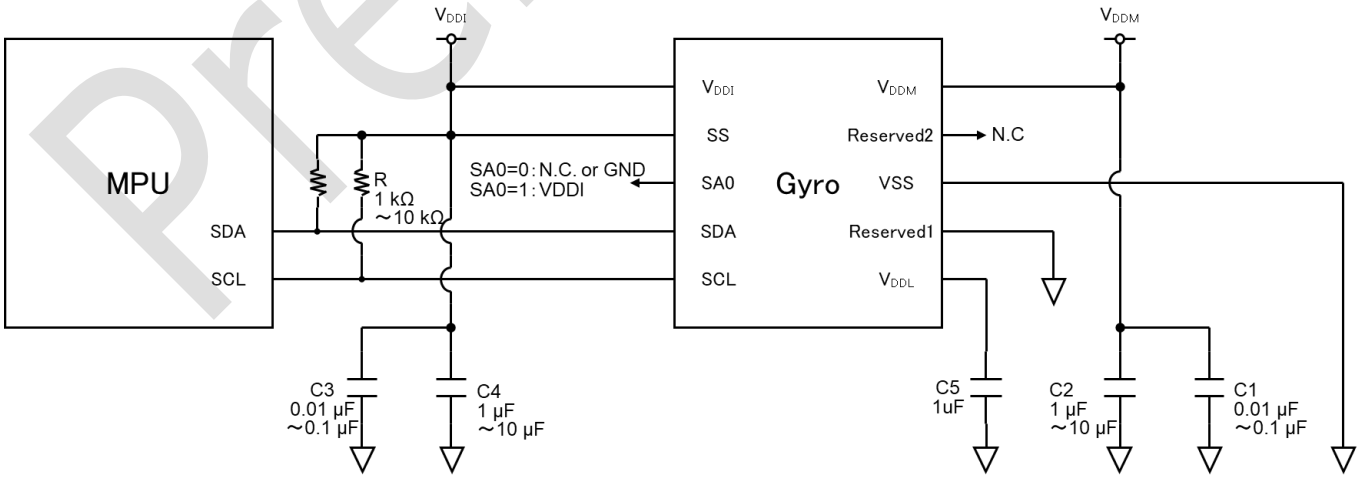


Figure 9.3 Example of I²C Connection

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10 Other information

10.1. Moisture Sensitivity Level (MSL)

Table 10.1 MSL

Parameter	Level	Standard
MSL	1	JEDEC J-SD-020D.01

10.2. Electro-Static Discharge (ESD)

Table 10.2 ESD

Model	Min.	Standard & Condition
HBM	2000 V	JESD22-A114, V_{DDM}, V_{DDI} and GND reference, 3 times
MM	200 V	JESD22-A115, V_{DDM}, V_{DDI} and GND reference, 1 time

10.3. Soldering Profile

A solder heat resistance of this product was verified under the air reflow soldering profile (JEDEC J-STD-020D.1) shown in Figure 10.1

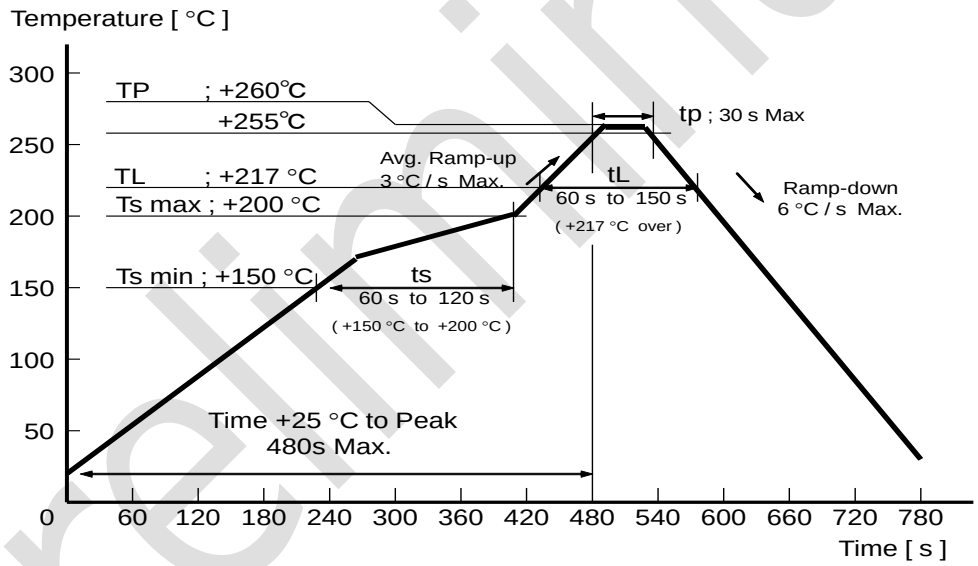


Figure 10.1 Soldering Profile

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11 Taping Information

11.1. Taping Quantity

TBD

11.2. Taping Specification

TBD

11.3. Taping Dimensions

TBD

11.4. Reel Dimensions

TBD

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12 Terminology

12.1. Cross Axis Sensitivity

The value is derived by dividing sensitivity around the X and Y axis by the sensitivity around the Z axis. The X, Y, and Z axis directions are as shown in Figure 12.1.

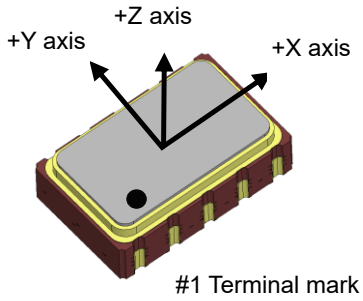


Figure 12.1 Each axis detection

12.2. Drive Frequency

The drive frequency is the resonance frequency (drive mode) of the sensor element continuously vibrated to gain the Coriolis force.

12.3. Detuning Frequency

The detuning frequency is the natural frequency used for the mechanical-electrical transduction of the Coriolis force. It is the difference from the drive frequency.

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13 Hnadling Precaution

Crystal devices are high precision products. Use the following precautions during handling.

1) The detuning frequency for this product is Typ 1000Hz. During board design, the customer must ensure that the board resonance frequency is not within the vicinity of this detuning frequency. When mounting on a board, align the sensor near a board loading component with low resonance variation.
2) Excessive shock from adsorption/chucking when mounting the sensor or excessive vibration or shock during board cutting or an impact wrench after mounting can result in damage to the sensor or the deterioration of sensor properties. Establish conditions that avoid vibration or shock to the sensor to ensure there is not loss in performance.
3) To detect angular rate, this product uses a drive frequency to drive the sensor element. External application of a signal with frequency components in the vicinity of the drive frequency or high-order harmonics can result in fluctuations in angular rate output by the sensor. Be sure to confirm internally in advance concerning power supply decoupling measures and serial interface communications frequency settings.
4) To prevent malfunctions caused by electromagnetic induction and static induction from other signal lines, during pattern design do not pass other signal lines near the sensor or along the back of the package. Also, use a pattern design that does not cross with other signal lines.
5) It may occur communication error with the device due to the signal pattern of board. In that case, please connect dumping resistor to reduce noise/overshoot/undershoot of the signal.
6) Confirm internally in advance concerning measures for vibration, shock, and noise.
7) This product design incorporates shock resistance but there is the risk of product damage due to drops and shock. **Do not use this product if it has been dropped as we cannot guarantee product performance.**
8) Applying ultrasonic vibration during ultrasonic washing can cause resonance damage to the crystal unit depending on usage conditions. As we cannot specify the usage conditions (washer type, power, time, tub position, etc.) at your company, we offer no guarantees concerning operability after the application of ultrasonic vibration. Confirm internally prior to use if the use of ultrasonic washing is required.
9) Prior to use, conduct mounting tests internally to confirm there is no impact on performance. Similarly, confirm prior to changing any conditions. During and after mounting, ensure that the sensor is not in contact with boards or structural elements.
10) The sensor includes a static electricity protection circuit, but application of significant static electricity can result in damage to the sensor's internal IC. Make sure to use conductive materials for packaging and transport containers as well. For the soldering iron, measurement circuit, etc., use products with no high-voltage leaks and during mounting make sure to employ static electricity measures such as the use of a ground wire.
11) Keep reflow to no more than three times. Use a soldering iron to correct any soldering mistakes. Here, the temperature of the iron type should be below +350 °C and less than 3 seconds. (Blower use not allowed)
12) We recommend using board production based on Epson pad dimensions.
13) This product has the same frequency noise as drive frequency. Remove using an appropriate filter circuit.
14) This product is designed to resist acoustic interference even when multiple sensors are operated in close proximity but impedance common to board resonance and power supply could result in mechanical or electrical interference. Confirm internally prior to use.
15) This product includes a POR circuit. To avoid the POR circuit malfunctions, power supply voltage rise should be conducted between 0.01 ms and 100 ms.
16) Do not use in high condensation or other environments prone to short circuits between terminals.
17) Using the drive frequency integral multiplier as communications clock may result in fluctuations in the angular rate output.
18) Acquiring angular rate data as a frequency that is a fraction of the integer for the drive frequency can result in fluctuations in the angular rate output.

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